Sequentiality and Determinacy for Reactive Systems

A Sequentially Constructive Circuit Semantics for Esterel

Alexander Schulz-Rosengarten,
Steven Smyth, Reinhard von Hanxleden, Kiel University
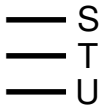and Michael Mendler, Bamberg University

Berry Constructive Circuits (BCC)

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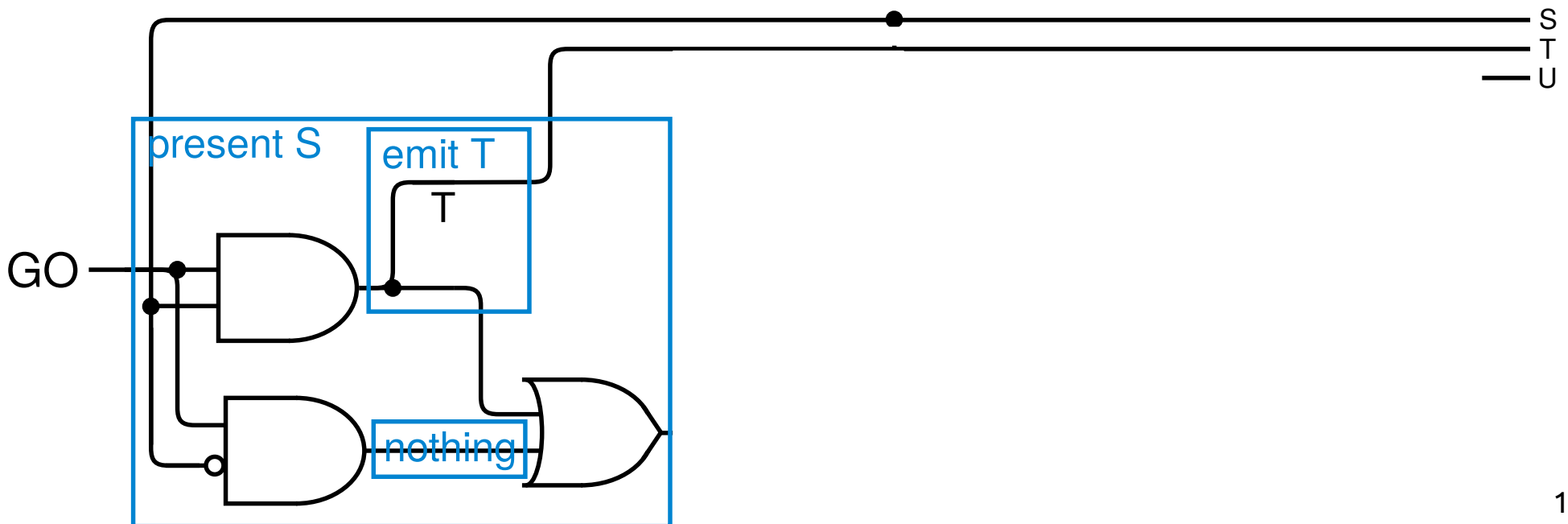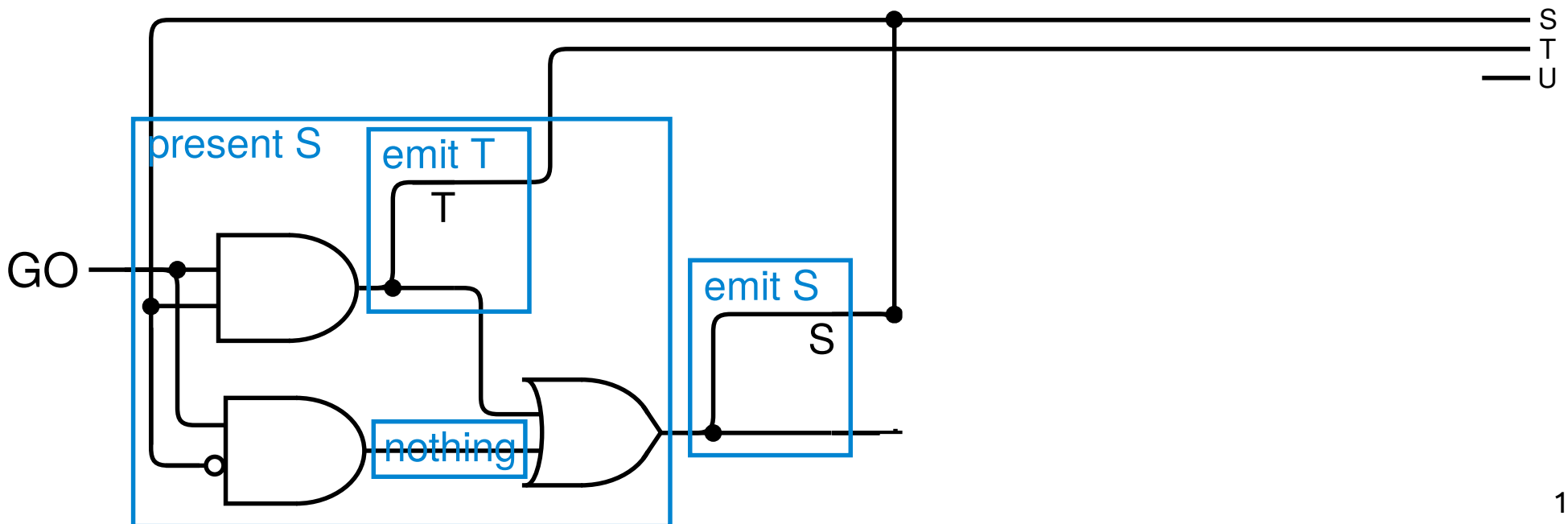
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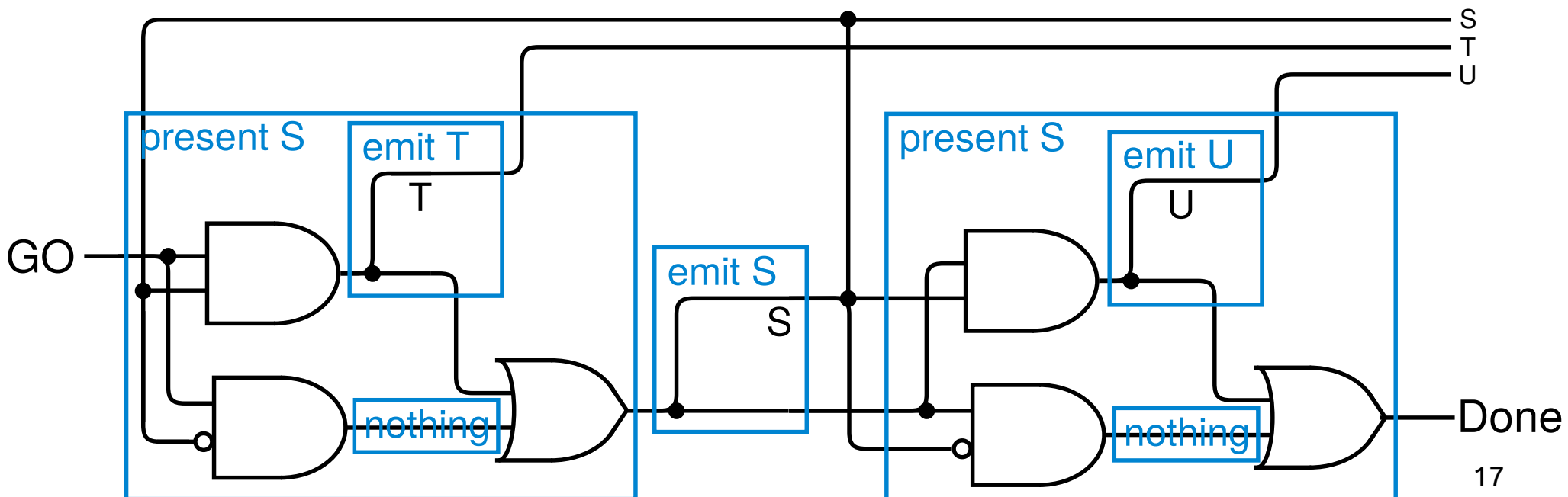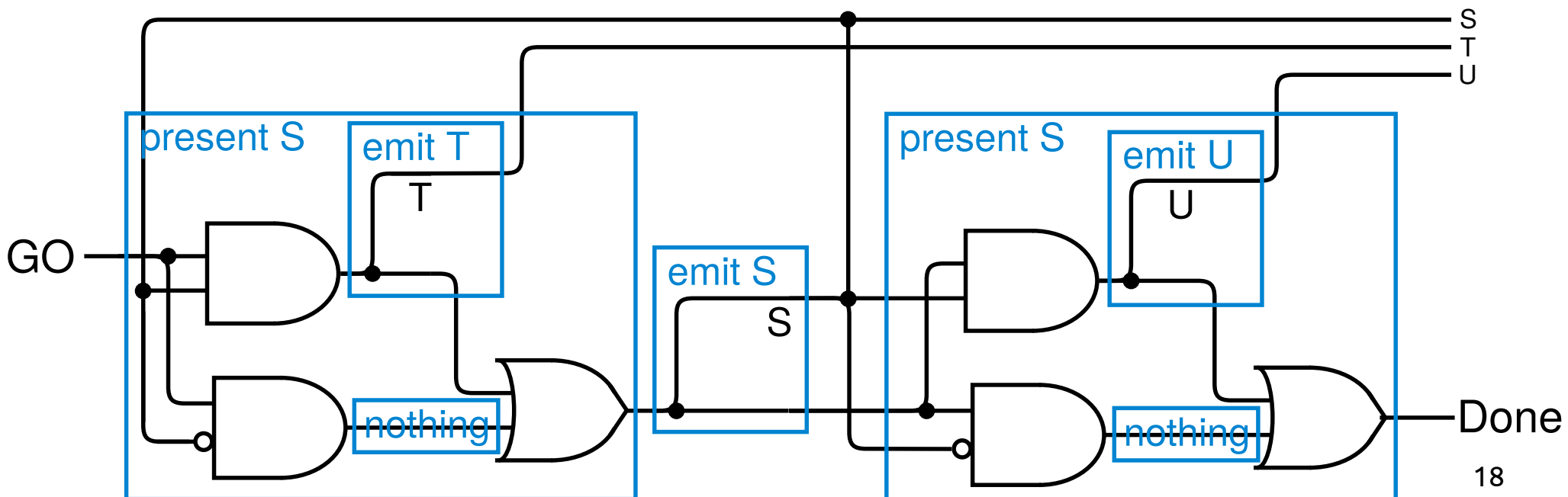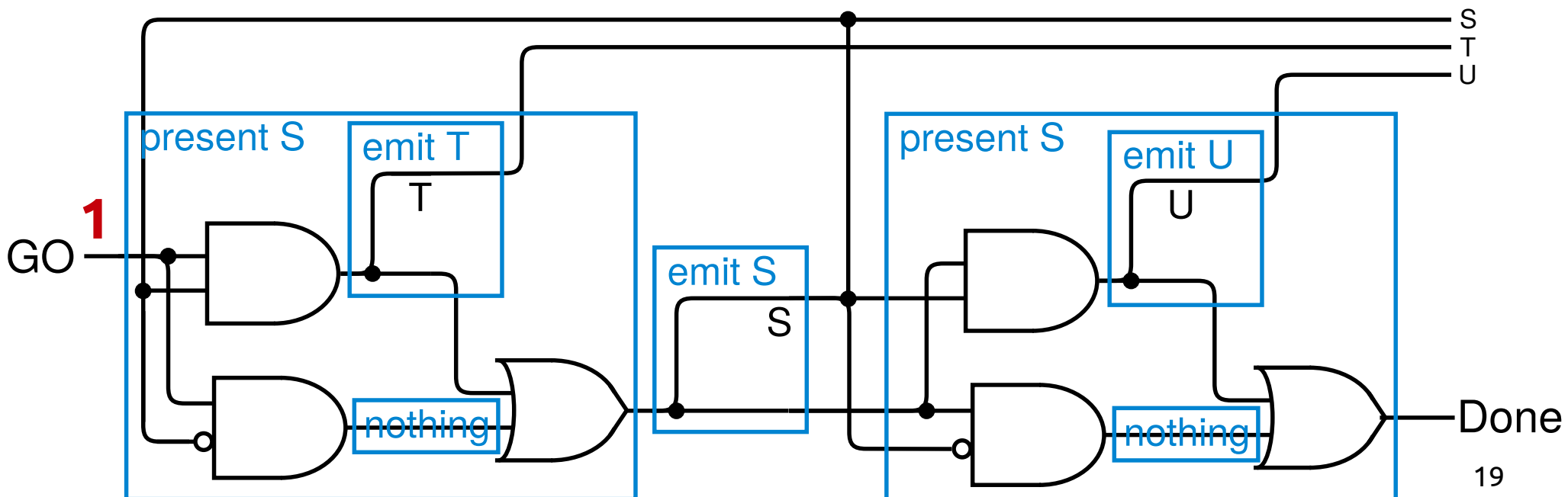
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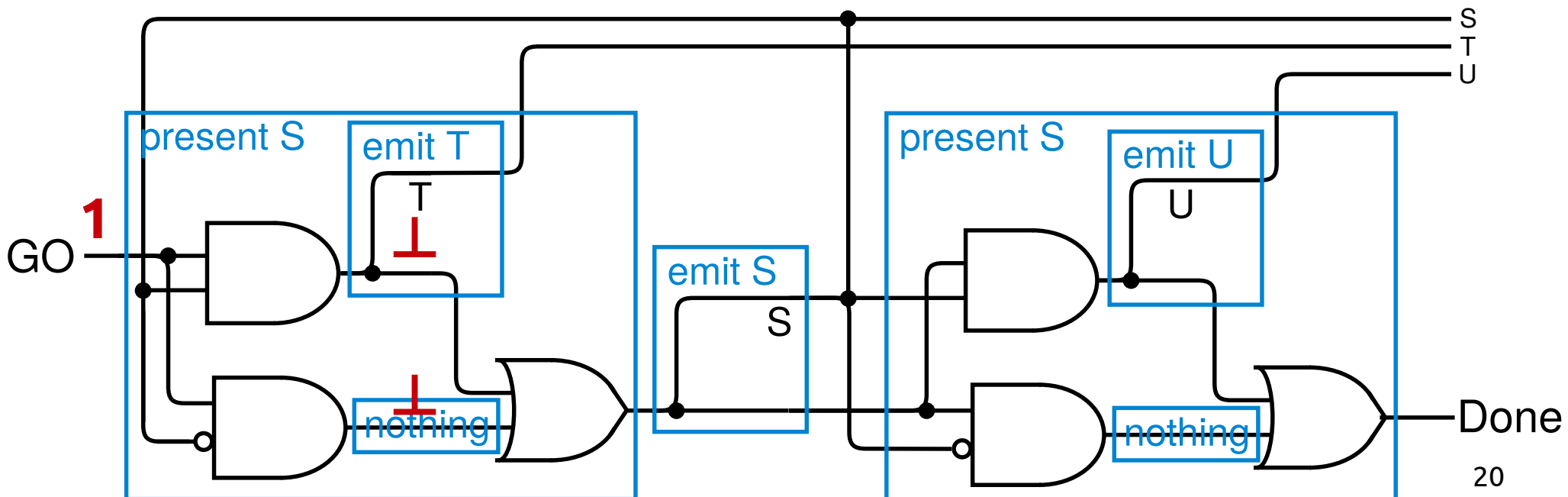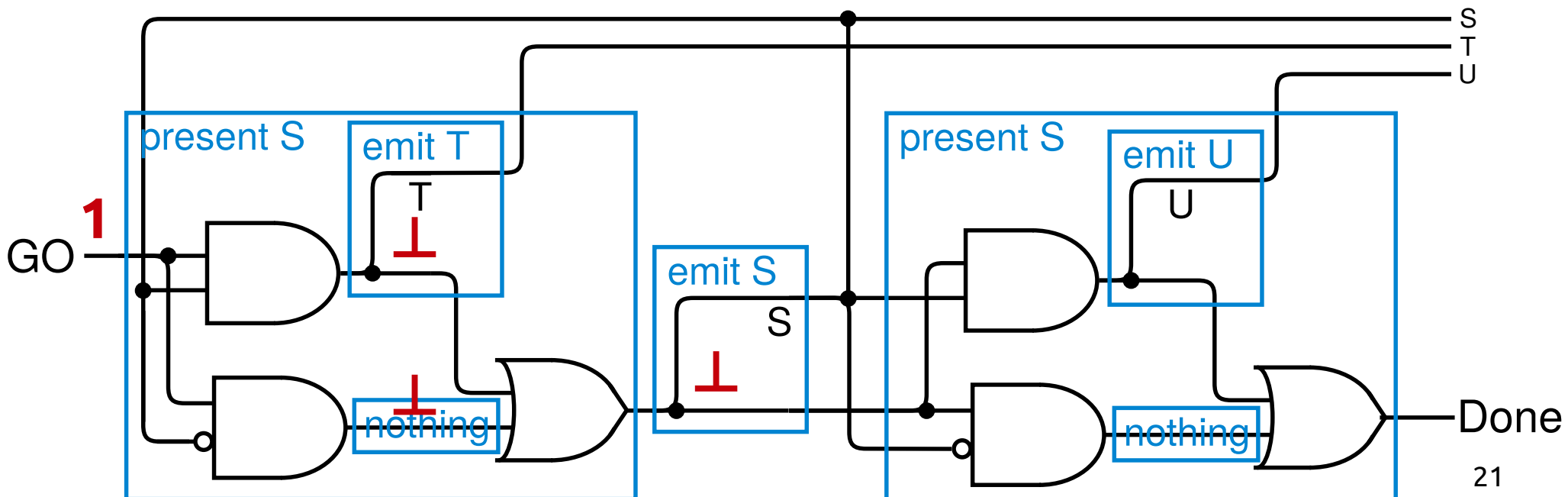
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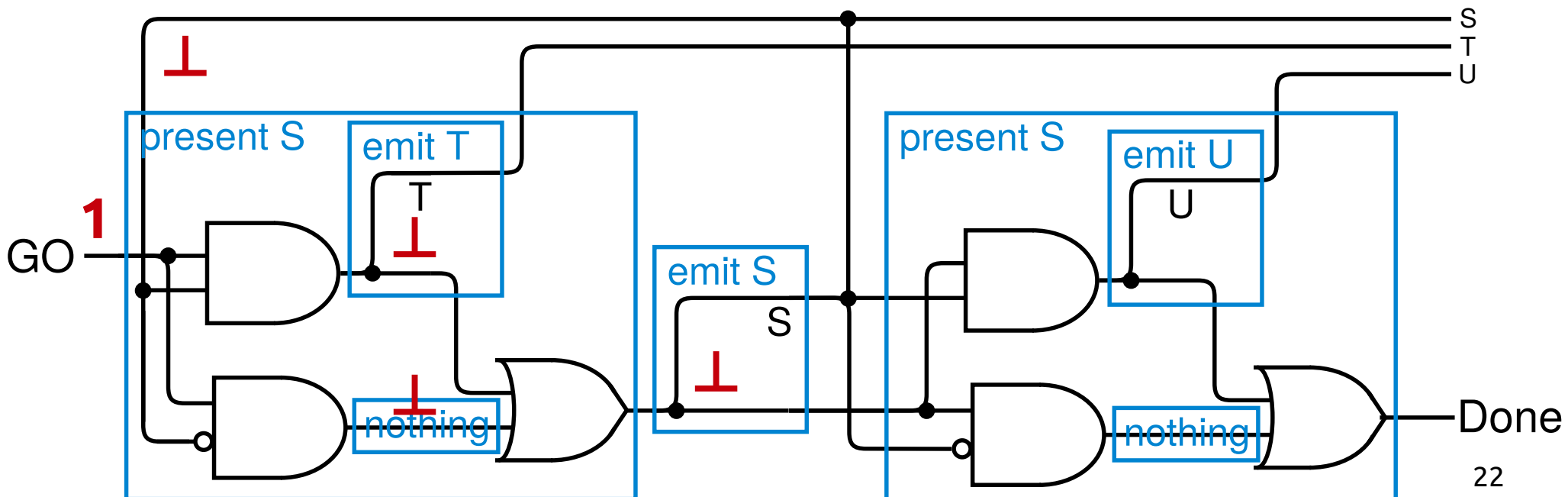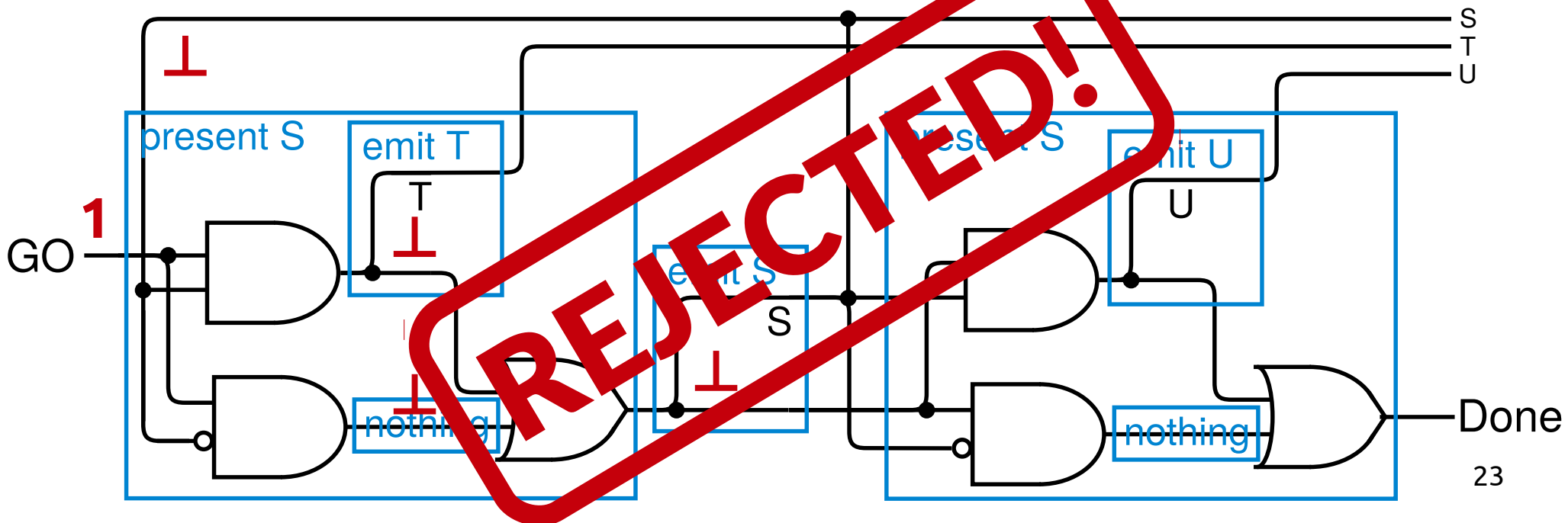

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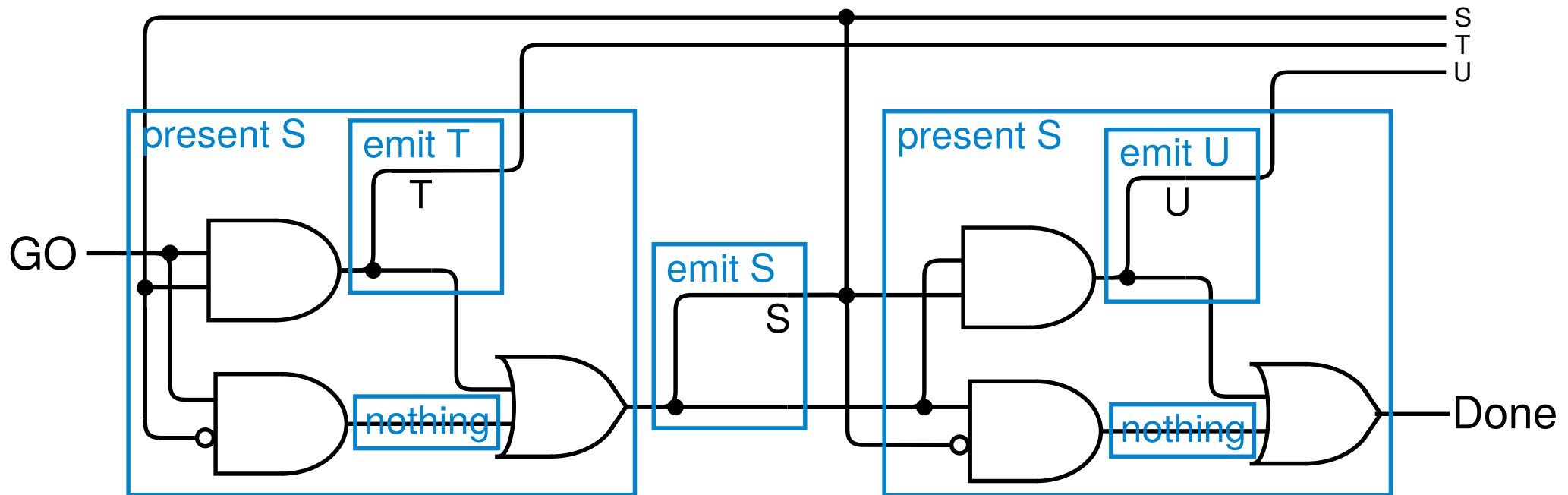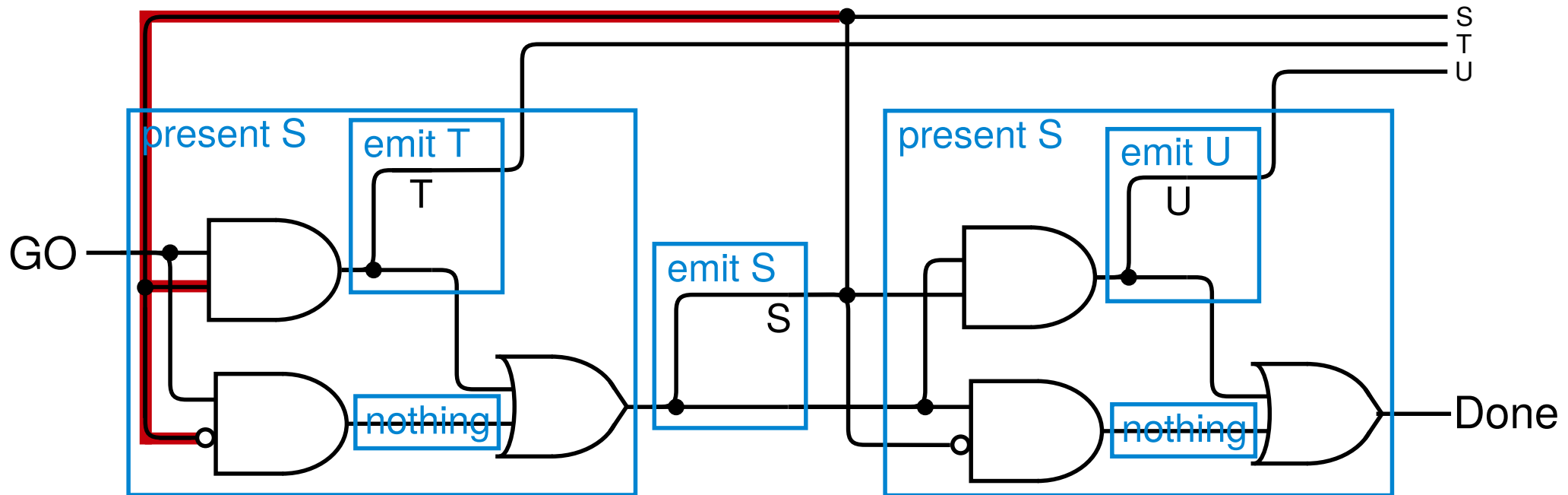*A signal is present/absent iff it must/cannot be emitted*

Sequentially Constructive Coherence Law:
A signal is present/absent iff it must/cannot be emitted
concurrently or sequentially preceding

We say that an emit E is **SC-visible** to a present test P if:
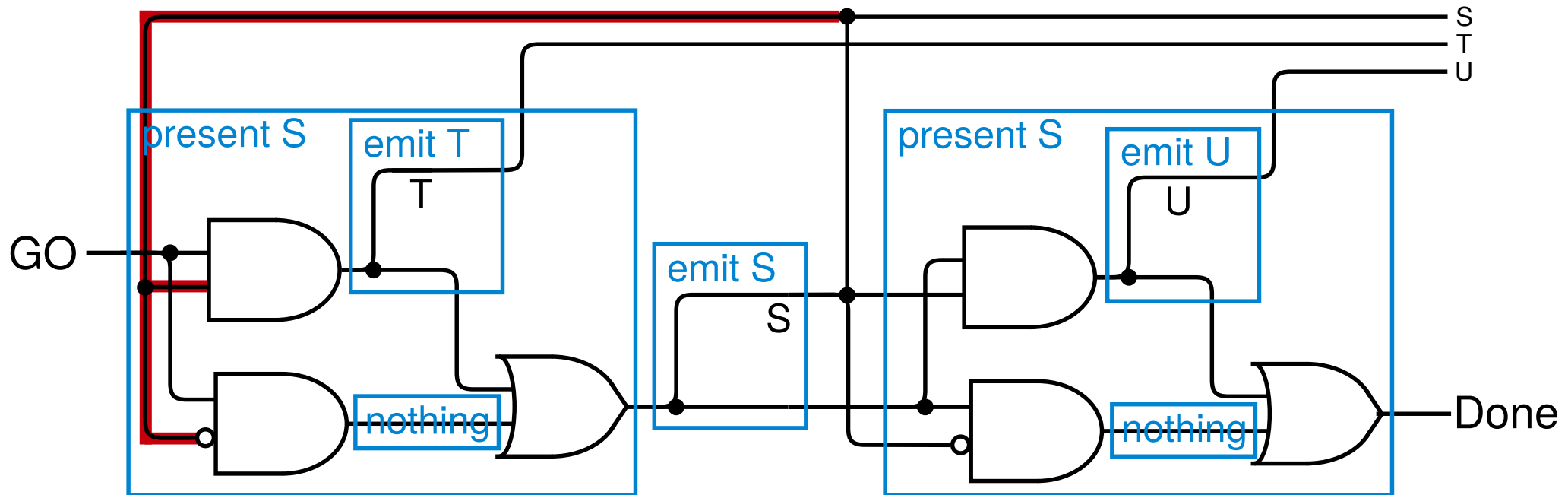1) E is concurrent to P or
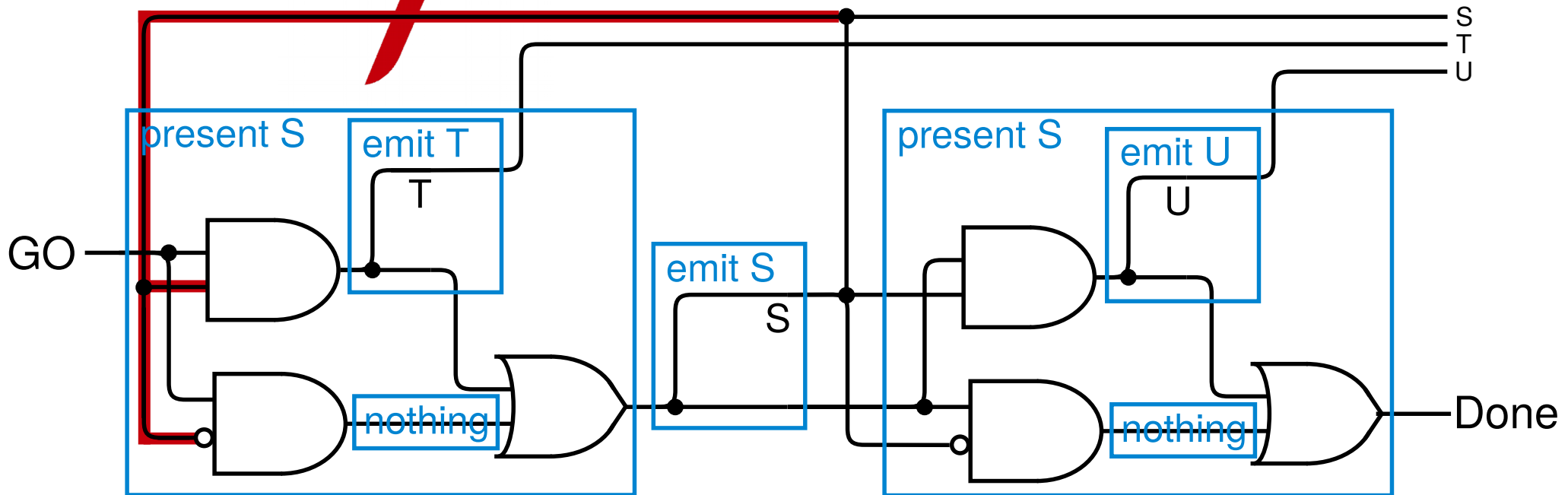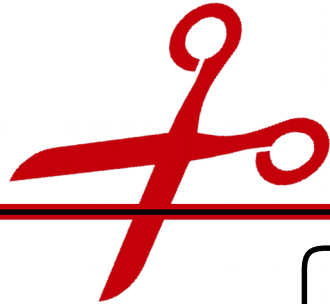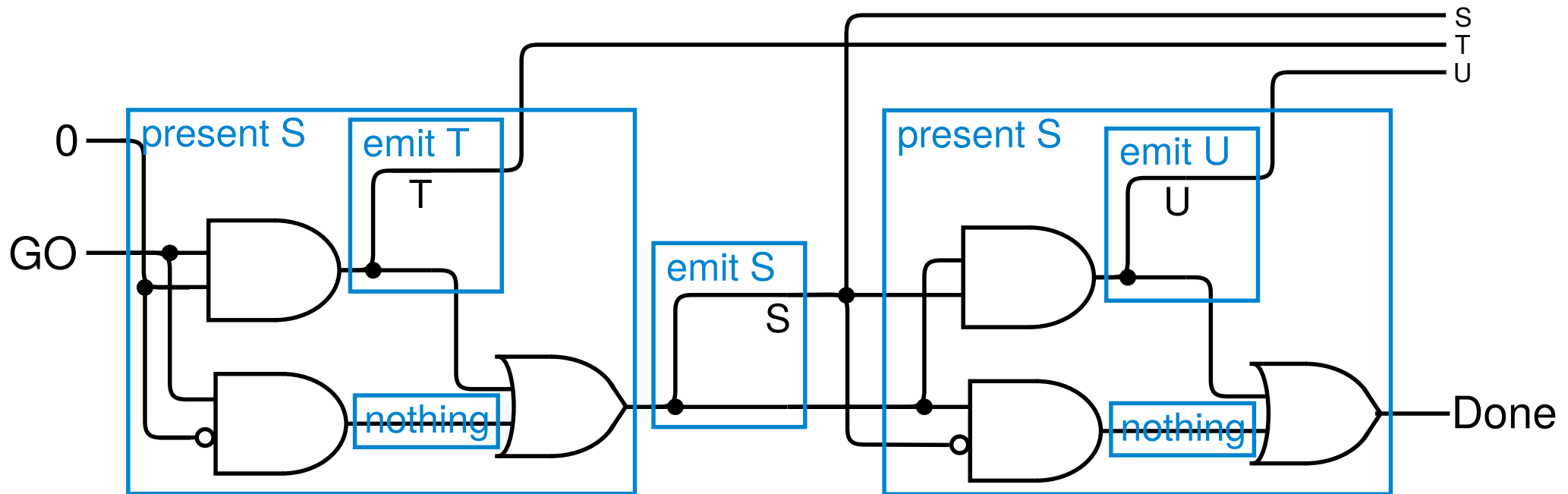2) E sequentially precedes P

SC-Visibility in Circuits

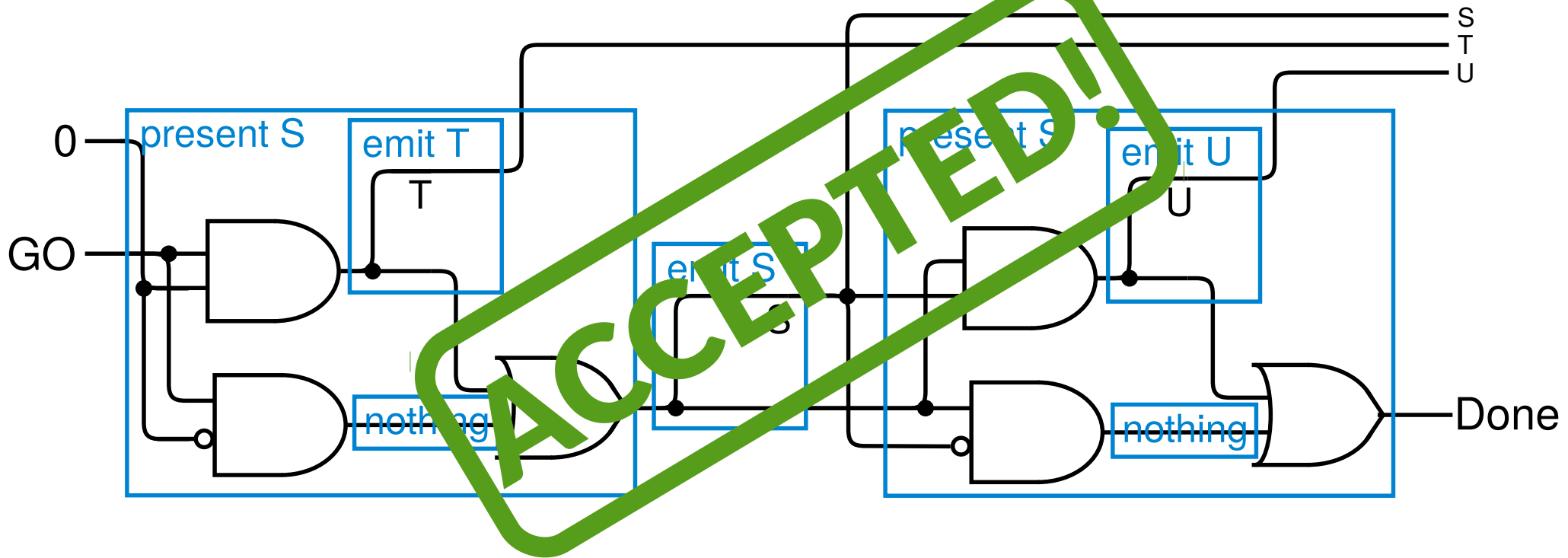# SC-Visibility in Circuits

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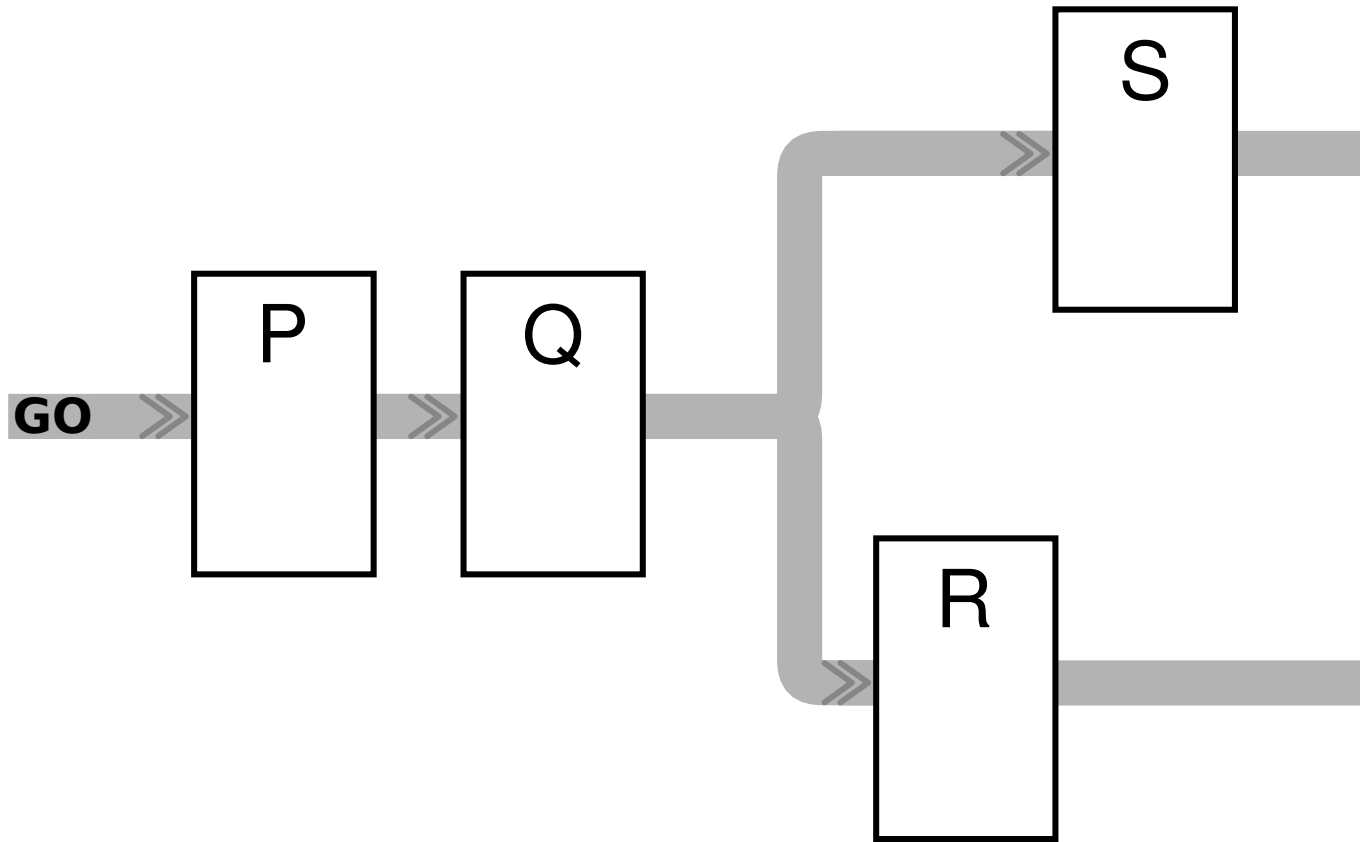# SC-Visibility in Circuits

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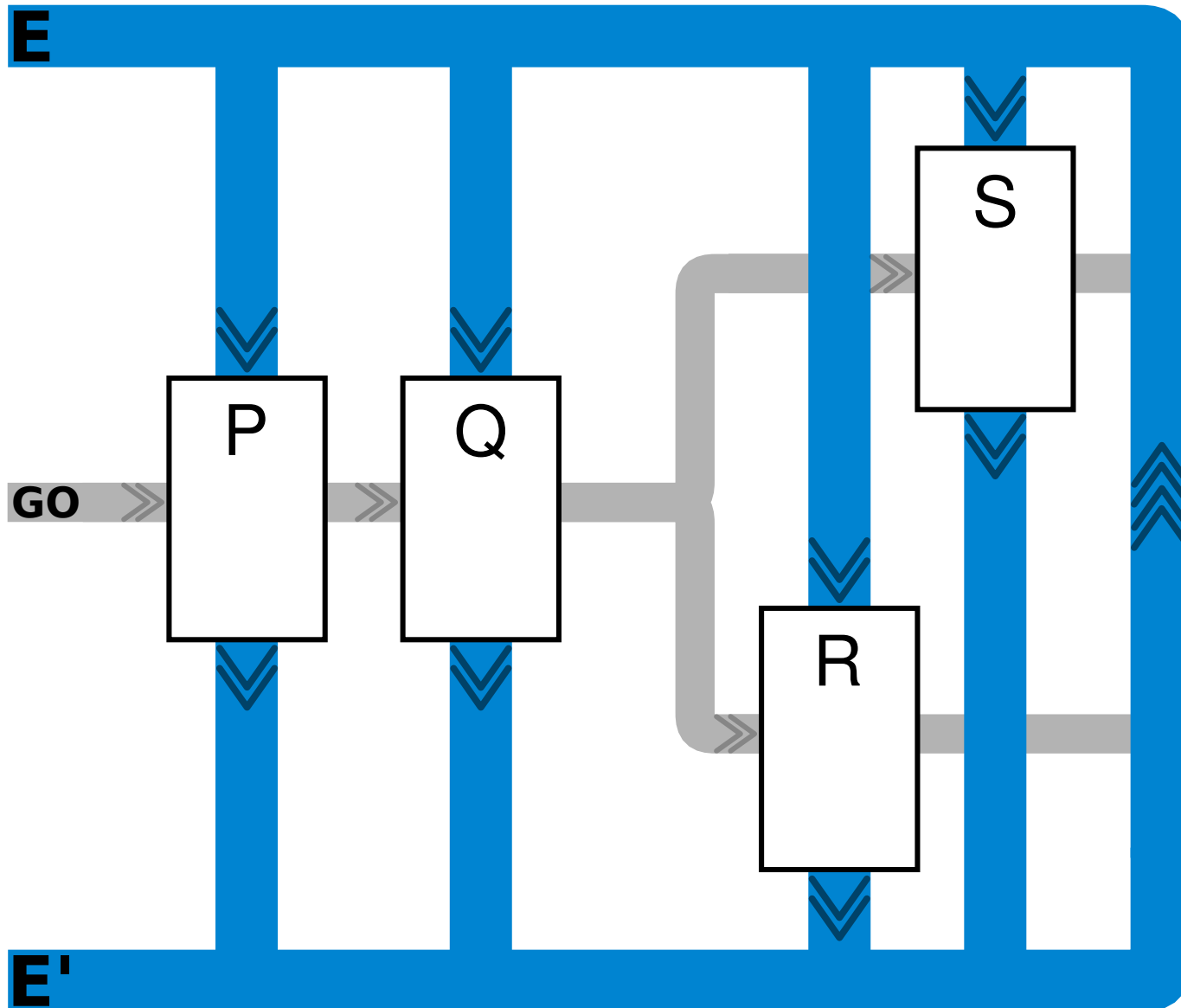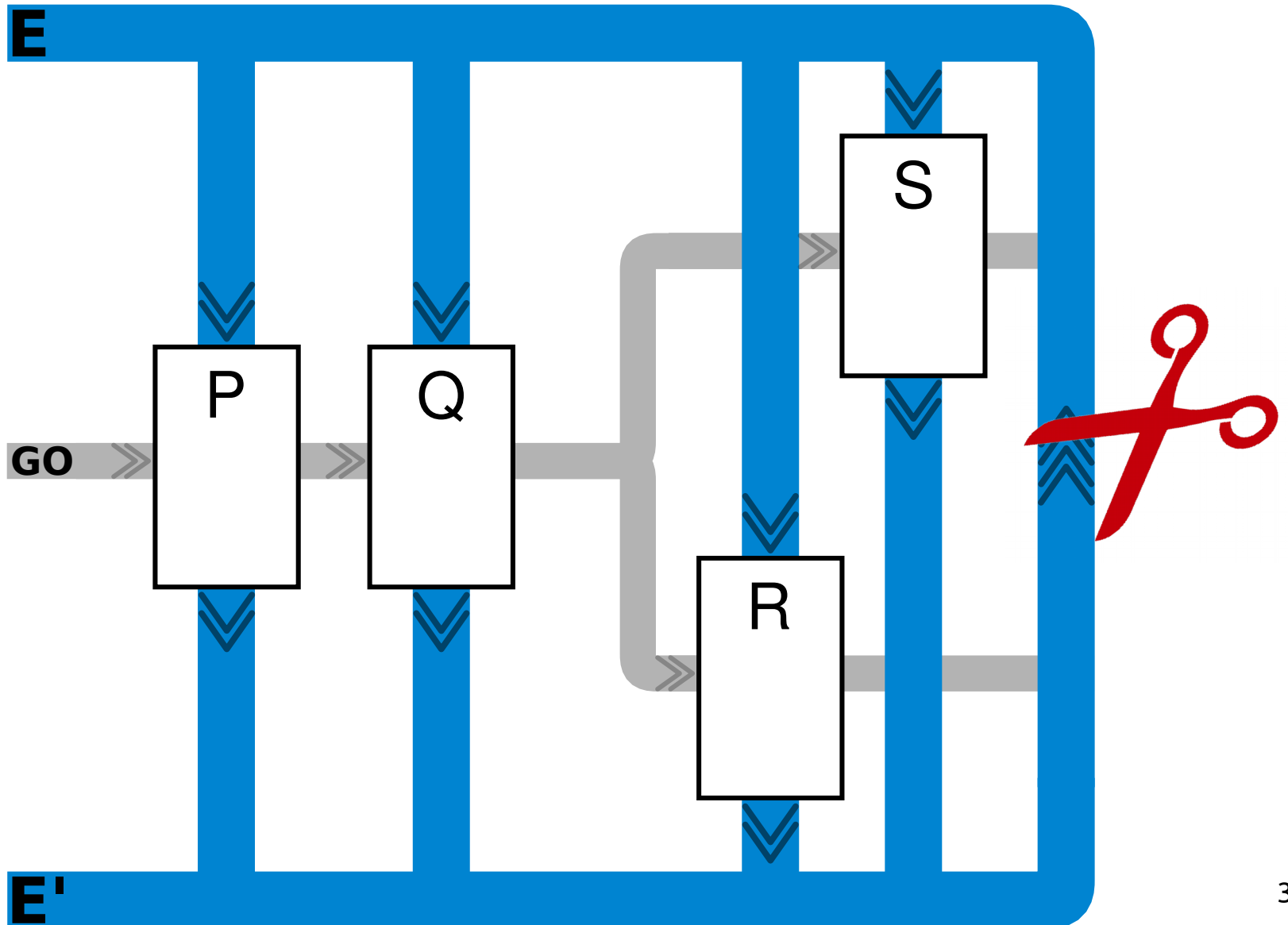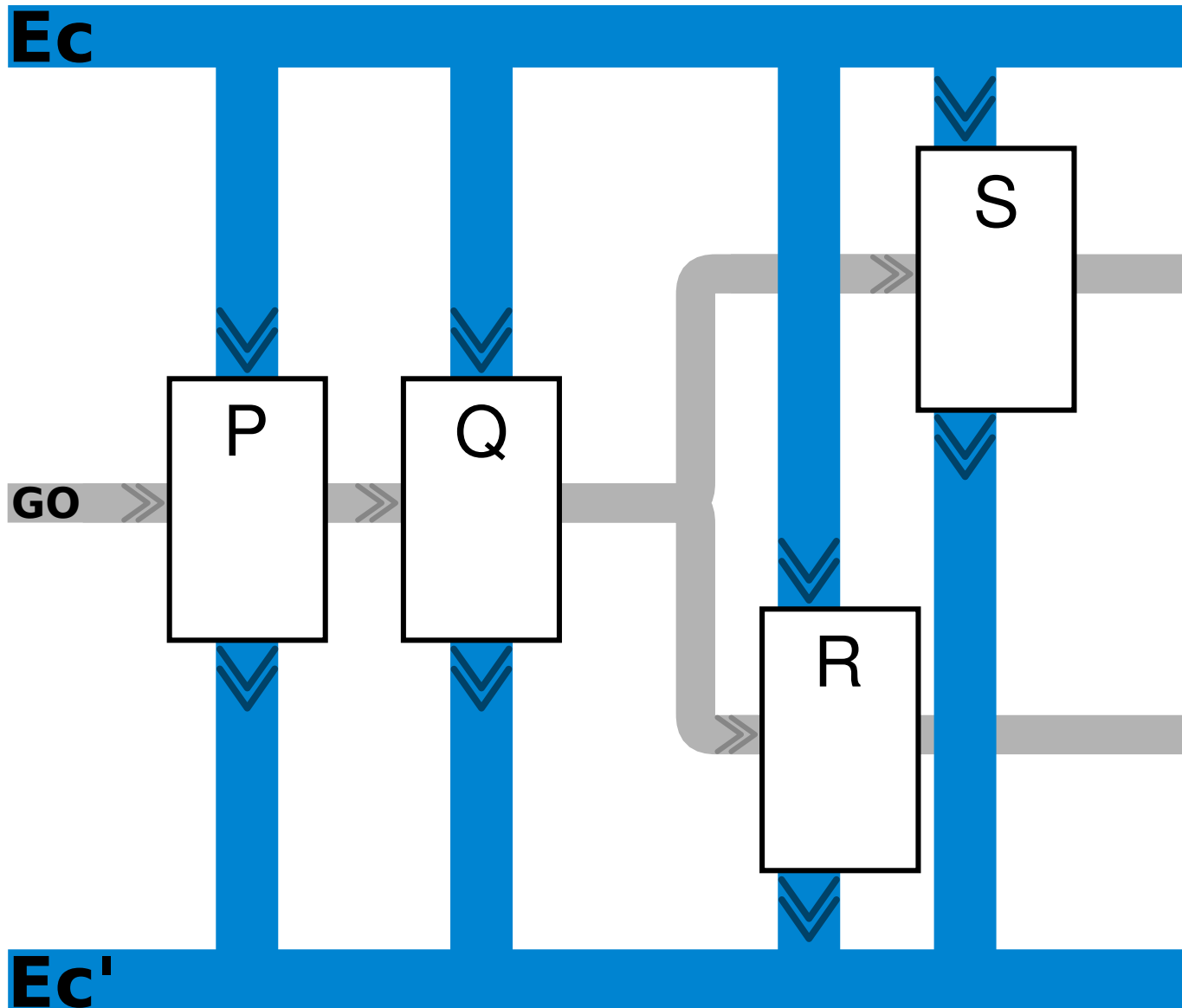# SC-Visibility in Circuit Construction
P ; Q ; [R ‖ S]

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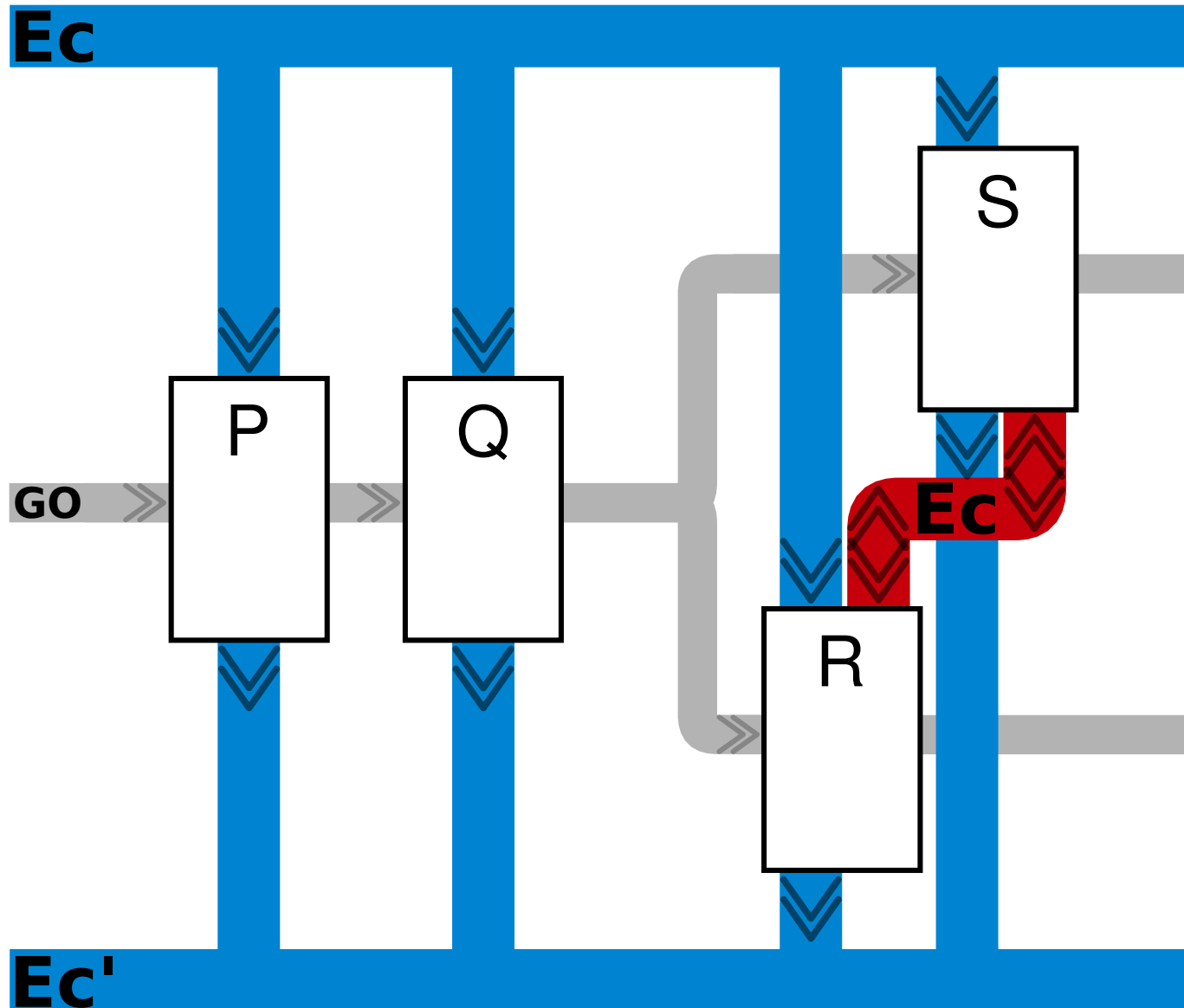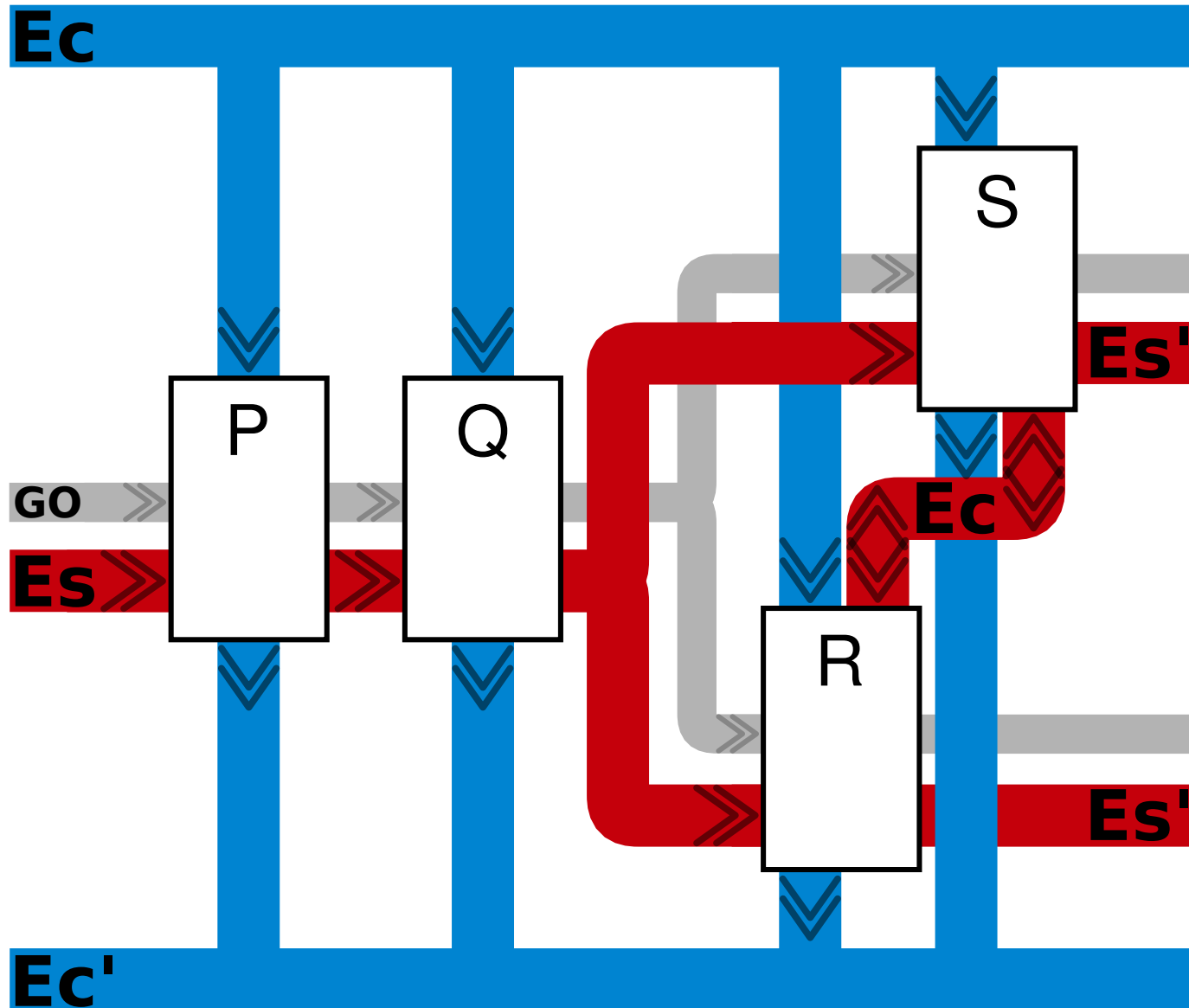# SC-Visibility in Circuit Construction
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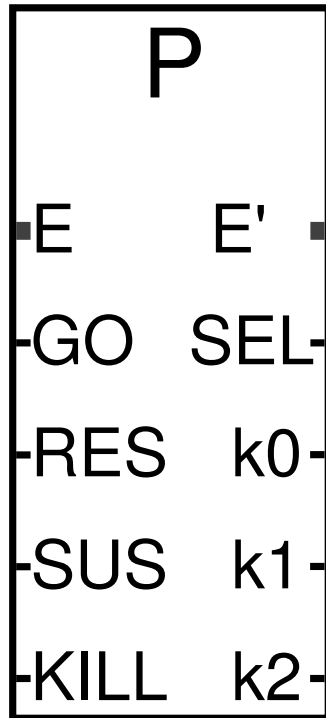# SC-Visibility in Circuit Construction
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Circuit Interface
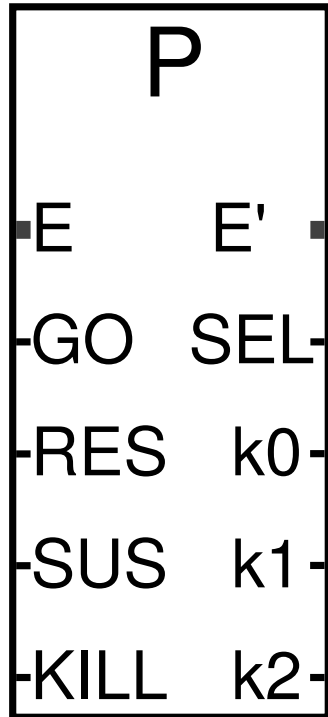
P

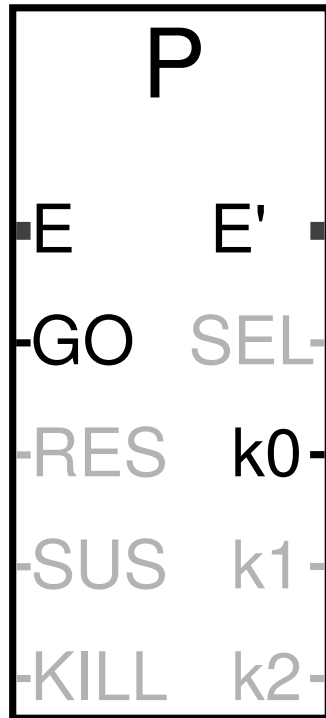| E | E' |
GO	SEL
RES	k0
SUS	k1
KILL	k2

Circuit Interface
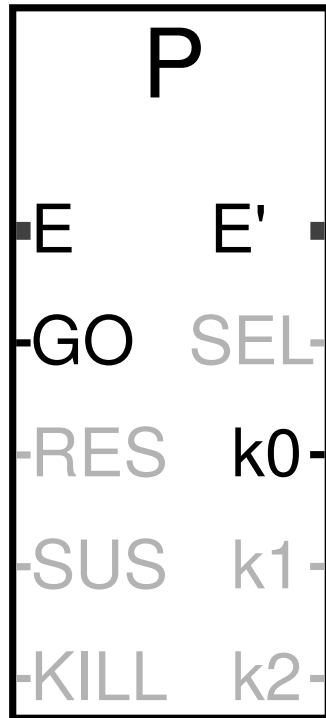

BCC
Berry Constructive
Circuit

Circuit Interface

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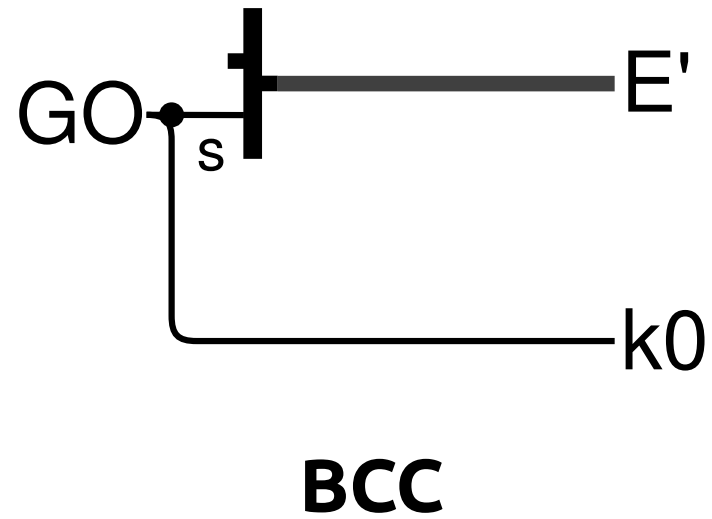Berry Constructive
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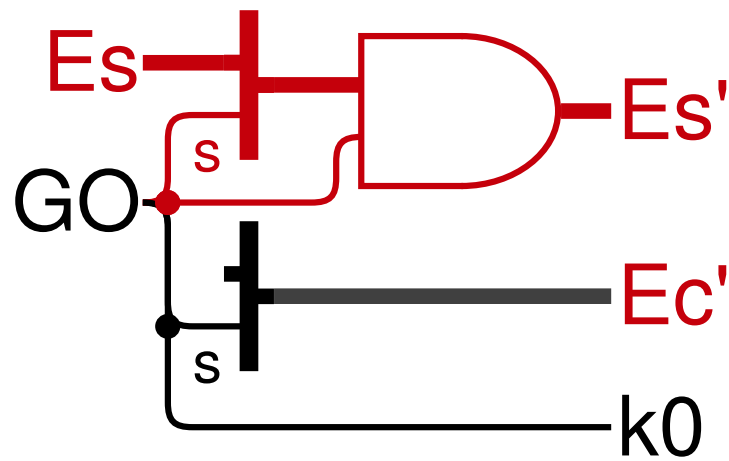Circuit

SCC
Sequentially Constructive
Circuit

emit s

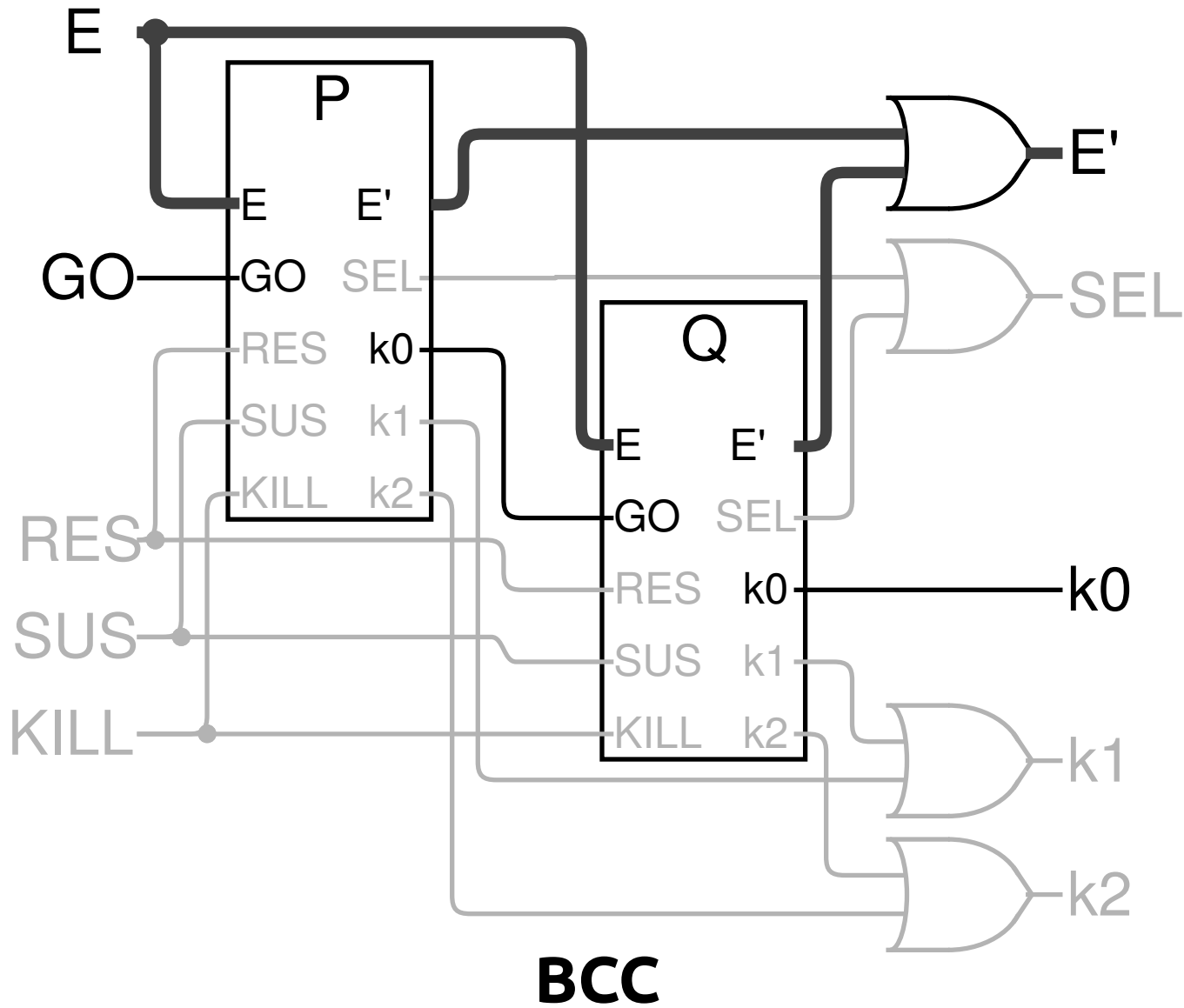GO—s—E'

—k0

BCC

emit s

scc

present s then P else Q

BCC

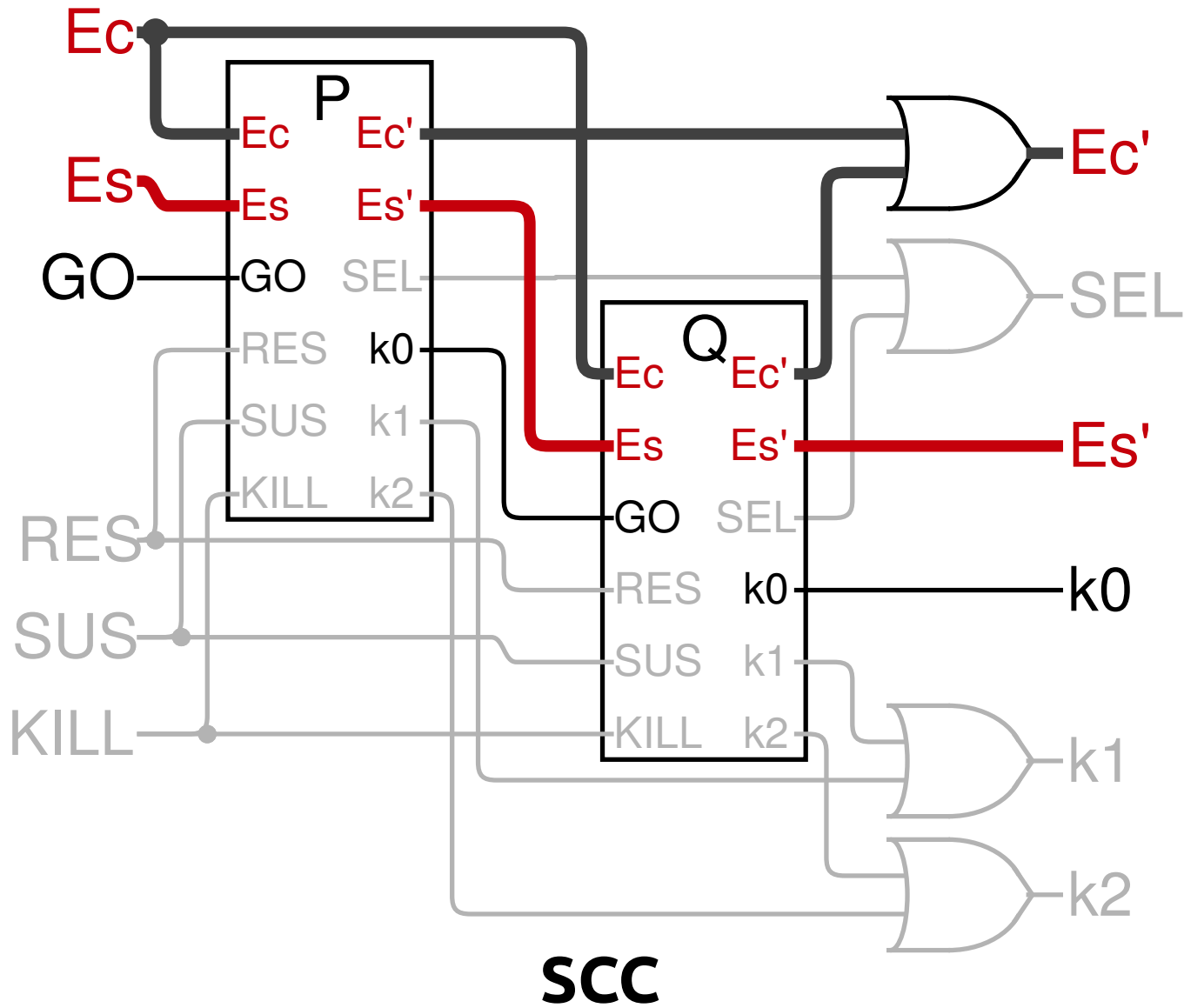# present s then P else Q

SCC

P ; Q

BCC

P ; Q

SCC
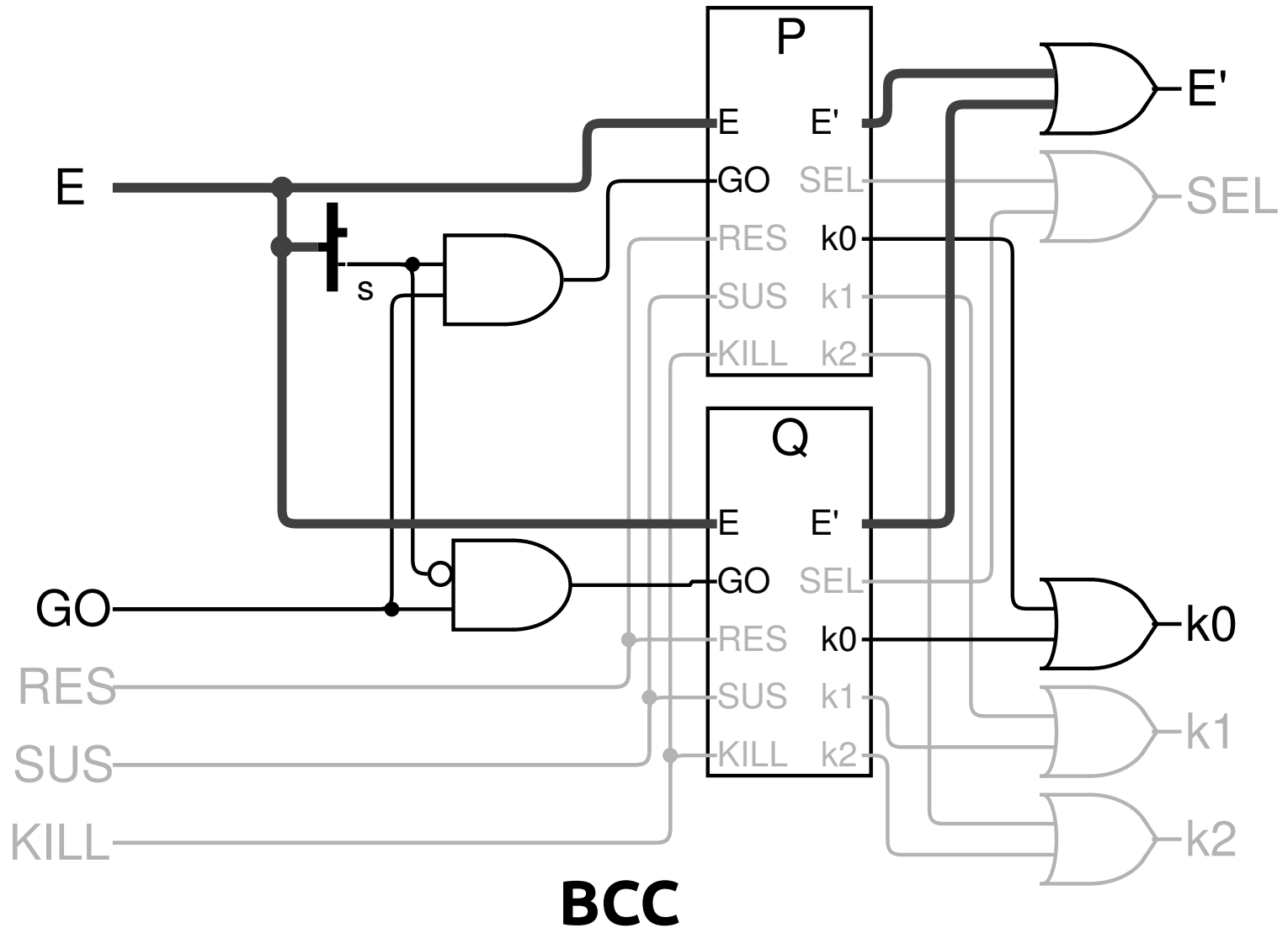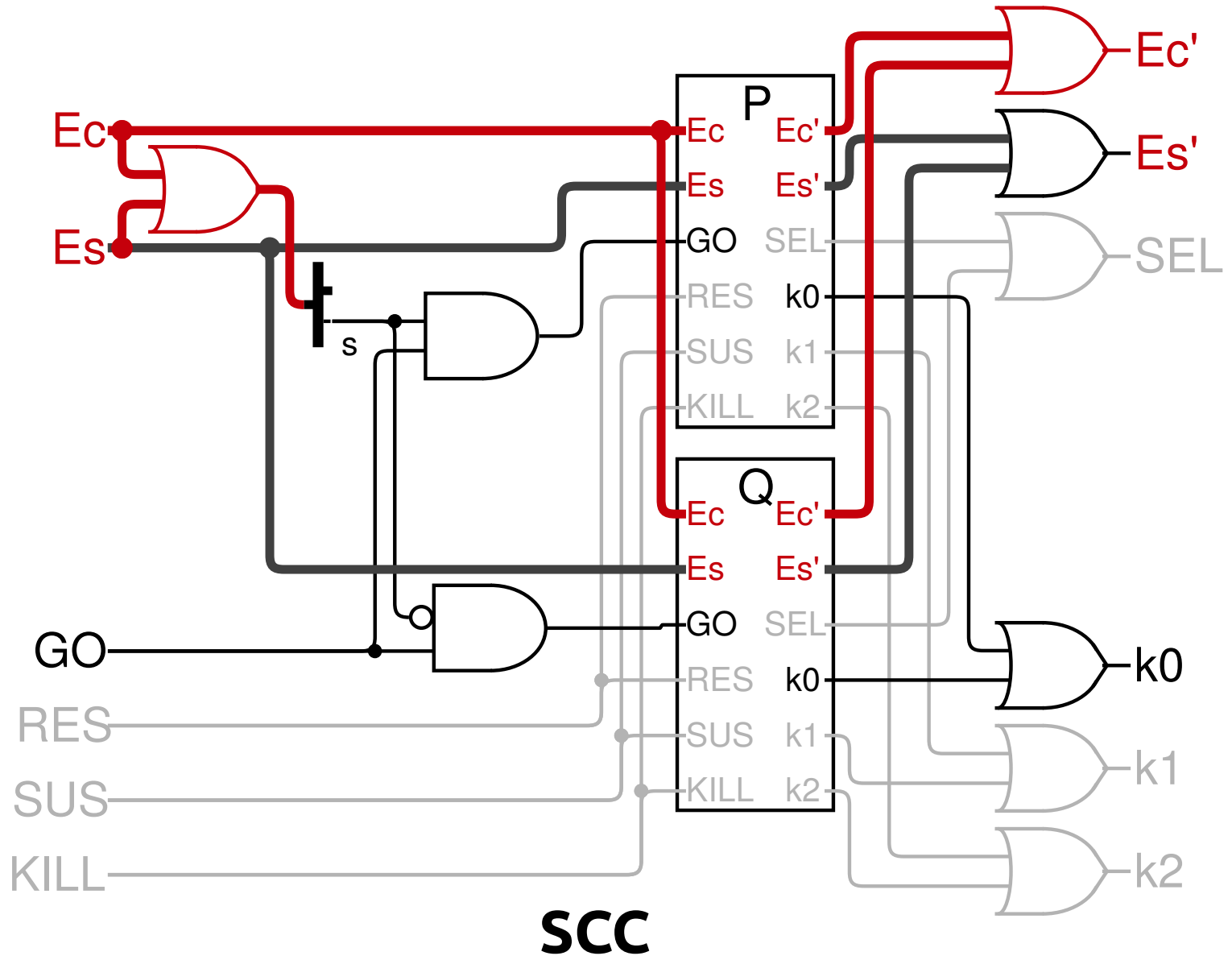
SCC Parallel
P || Q

Further SCC Rules

Signal

Loop

Pause

Exit

GO—k2

Nothing

Suspend

Trap

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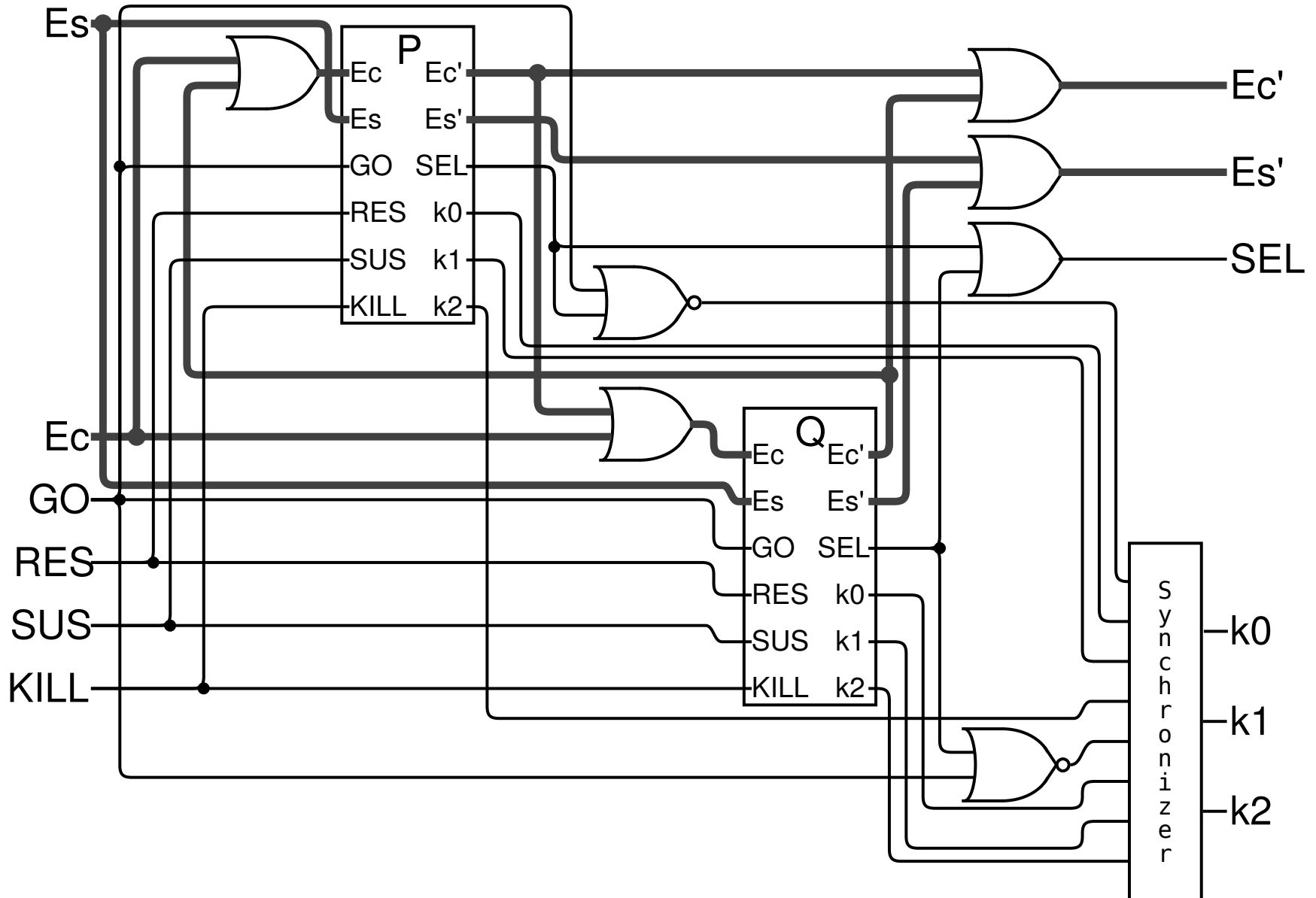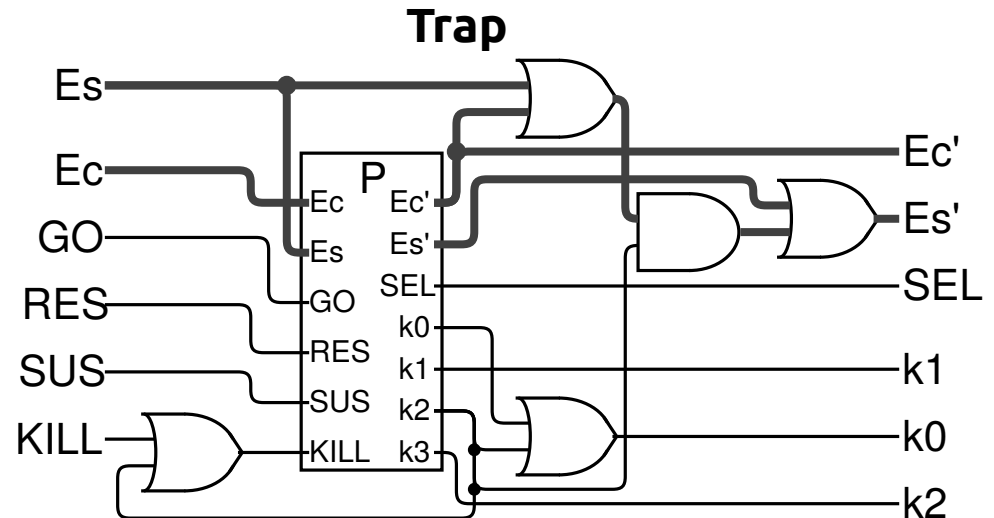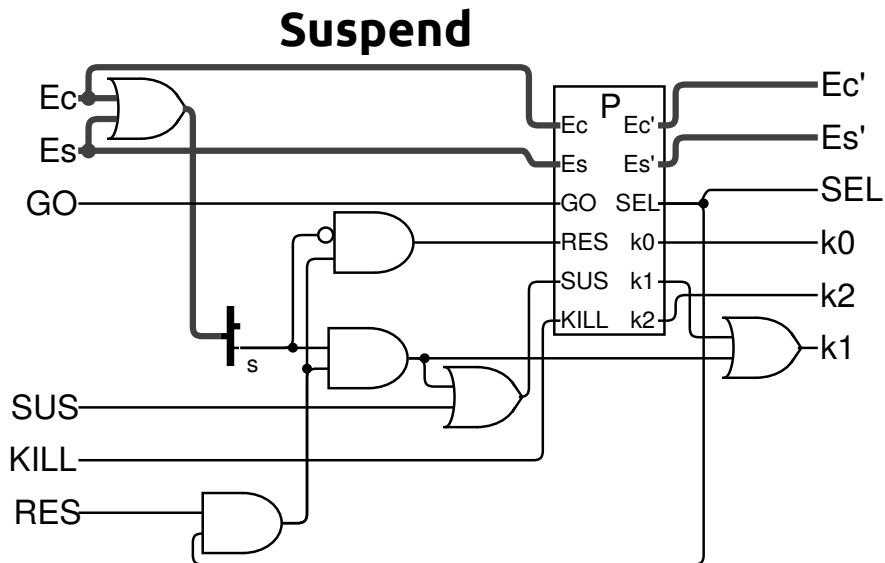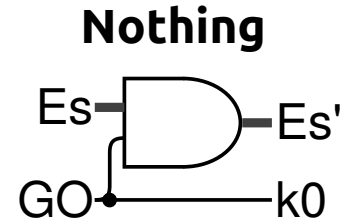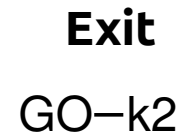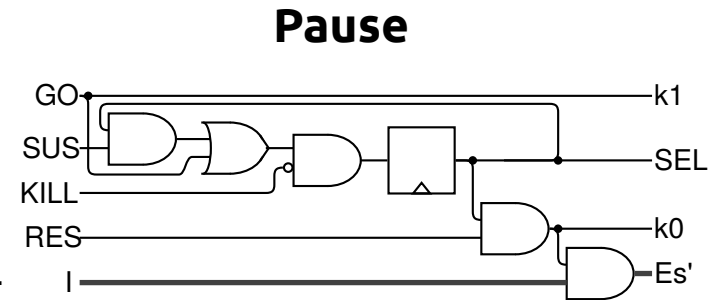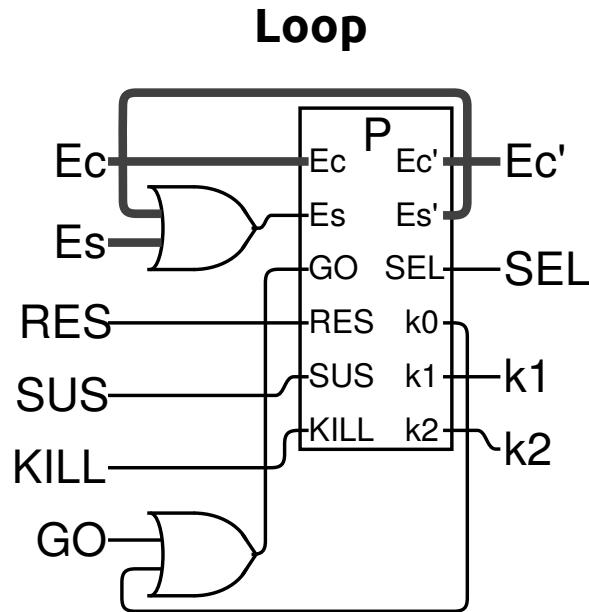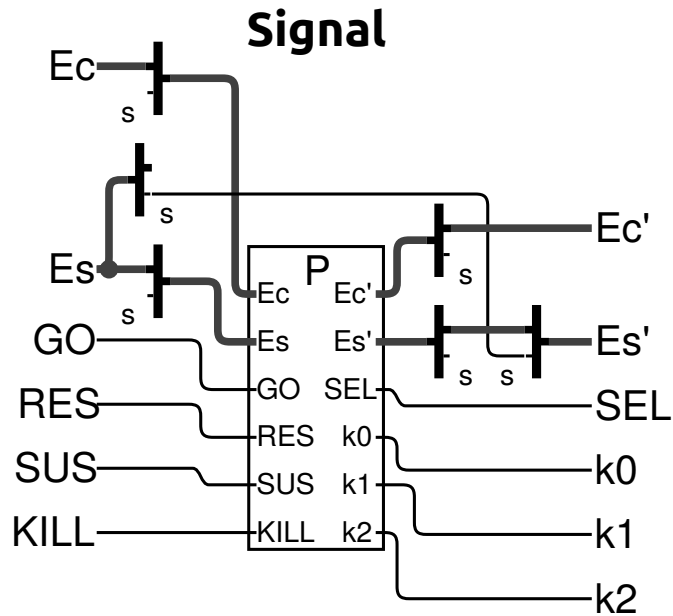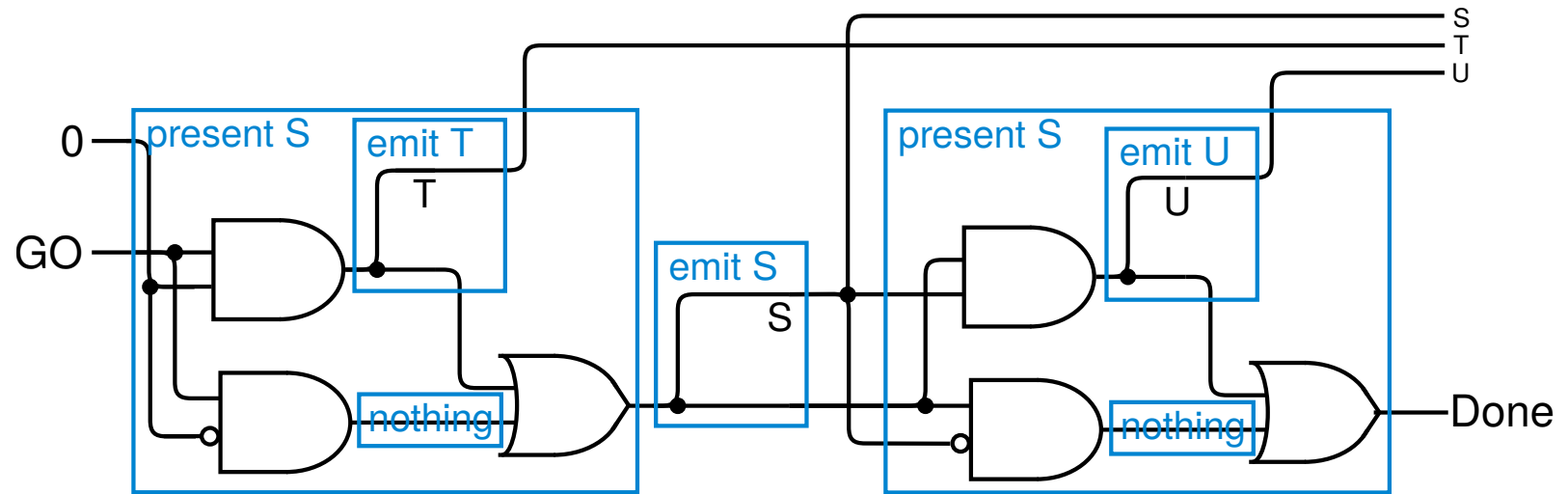
OffOn with SCC

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Formal Semantics and Conservativeness

Behavior of BC circuit with SC-visibility evaluation
$\Rightarrow$ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801[1])

[1] *A. Schulz-Rosengarten, S. Smyth, R. von Hanxleden, and M. Mendler, "A sequentially constructive circuit semantics for Esterel," Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1801, Feb. 2018, ISSN 2192-6247.*

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Evaluation Relation:
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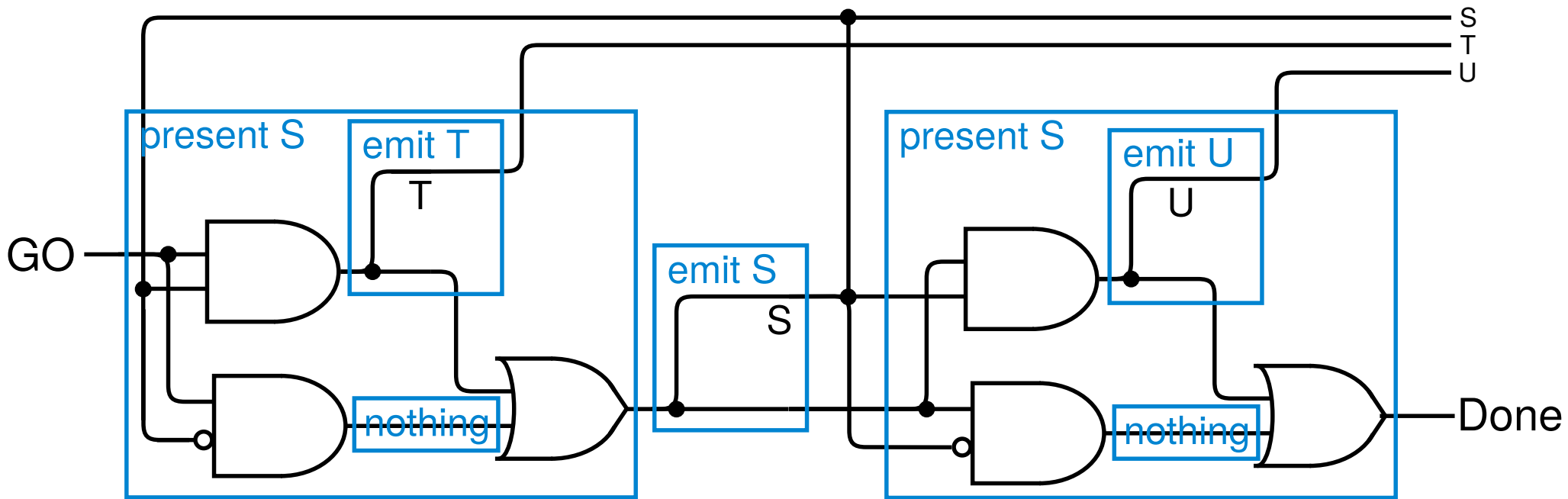*(Proof sketch in Technical Report 1801[1])*

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Evaluation Rules:

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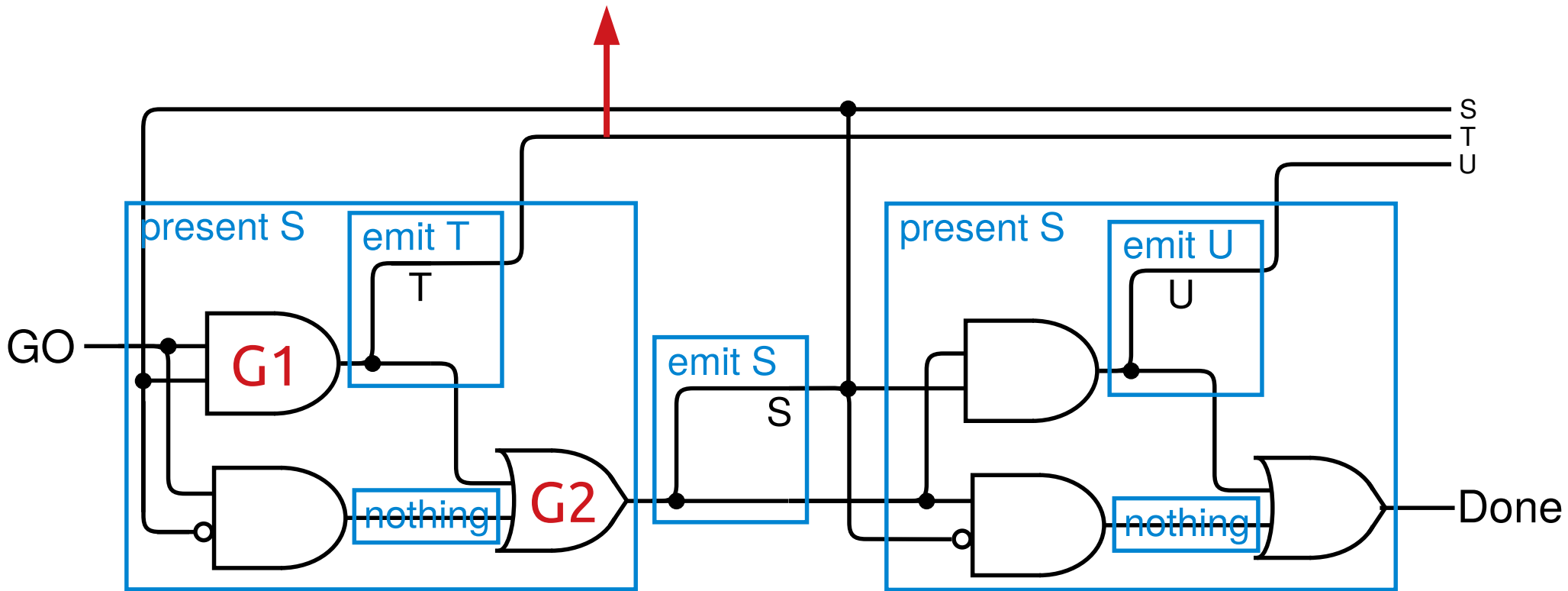
$$\frac{\forall w \Leftarrow_l e \in \mathcal{C}.\ \pi \npreceq l \Rightarrow e \hookrightarrow_{\pi \oplus l} 0}{w \hookrightarrow_{\pi} 0} ABS(\pi, w)$$

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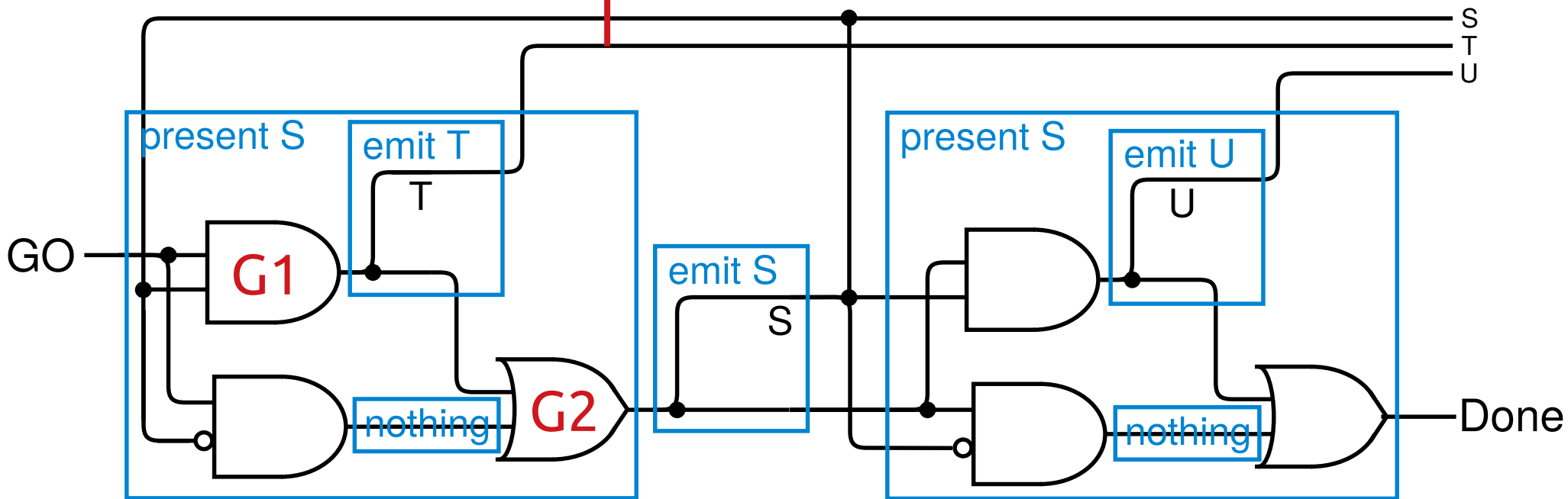
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$$T[G1] \iff GO \wedge S[G_2]$$

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$$T[G1] \;\Leftarrow\; GO \wedge S[G_2]$$

$$G1 \preceq G2 \;\Rightarrow\; S[G2] \hookrightarrow 0$$

Weak Unemit Circuit