Sequentiality and Determinacy for Reactive Systems

A Sequentially Constructive Circuit Semantics for Esterel

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Berry Constructive Circuits (BCC)

```plaintext
module OffOn:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```
Berry Constructive Circuits (BCC)

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Constructive coherence law:
A signal is present/absent iff it must/cannot be emitted
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GO-
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GO

Present S

emit T

T

nothing

Present S

emit S

S

nothing

Present S

emit U

U

nothing

Done

1
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REJECTED!
Proposal

Recall:
Constructive coherence law:
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**Sequentially** Constructive Coherence Law:
A signal is present/absent iff it must/cannot be emitted concurrently or sequentially preceding
Proposal

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**Sequentially** Constructive Coherence Law:
A signal is present/absent iff it must/cannot be emitted concurrently or sequentially preceding

We say that an emit E is **SC-visible** to a present test P if:
1) E is concurrent to P or
2) E sequentially precedes P
SC-Visibility in Circuits
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![Diagram of SC-Visibility in Circuits]
SC-Visibility in Circuits
SC-Visibility in Circuits
SC-Visibility in Circuits
SC-Visibility in Circuit Construction

\[ P ; Q ; [ R \parallel S ] \]
SC-Visibility in Circuit Construction

$P ; Q ; [ R \parallel S ]$
SC-Visibility in Circuit Construction

$P ; Q ; [ R \parallel S ]$

Diagram showing a circuit with nodes P, Q, R, S, E, and E'. There are connections between these nodes with a cut indicated by scissors at the connector of R and S.
SC-Visibility in Circuit Construction

$P ; Q ; [ R \parallel S ]$
SC-Visibility in Circuit Construction

\[ P ; Q ; [ R \parallel S ] \]
SC-Visibility in Circuit Construction
P ; Q ; [ R || S ]
Circuit Interface

P
- E  E'
- GO  SEL
- RES  k0
- SUS  k1
- KILL  k2
Circuit Interface

BCC
Berry Constructive Circuit
Circuit Interface

BCC
Berry Constructive Circuit
Circuit Interface

**BCC**
Berry Constructive Circuit

**SCC**
Sequentially Constructive Circuit
emit $s$

![Diagram of BCC with labels GO, E', k0, and BCC]
emit $s$
present s then P else Q
present s then P else Q
P ; Q

\[
\begin{align*}
E_c & \quad E_c' \\
E_s & \quad E_s' \\
G_O & \quad G_O \\
R_E & \quad R_E \\
S_U & \quad S_U \\
K_I & \quad K_I \\
\end{align*}
\]
SCC Parallel

\[ P \parallel Q \]
Further SCC Rules
OffOn with SCC
OffOn with SCC

[Diagram of a circuit with logical gates and annotations for present, emit, and nothing states]
Formal Semantics and Conservativeness

Behavior of BC circuit with SC-visibility evaluation
⇒ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801¹)

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Evaluation Relation:

\[ C, I, R \vdash e \rightarrow_\pi b \]
Formal Semantics and Conservativeness

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⇒ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801)

Evaluation Relation:

\[ C, I, R \vdash e \rightarrow_{\pi} b \]

Evaluation Rules:

\[ \exists w \leftarrow_{l} e \in C. \pi \not\leftrightarrow l \land e \rightarrow_{\pi \oplus l} 1 \]

\[ w \rightarrow_{\pi} 1 \quad PRES(\pi, l) \]

\[ \forall w \leftarrow_{l} e \in C. \pi \not\leftrightarrow l \Rightarrow e \rightarrow_{\pi \oplus l} 0 \]

\[ w \rightarrow_{\pi} 0 \quad ABS(\pi, w) \]
Formal Semantics and Conservativeness

G O

present S emit T

emit S

present S emit U

nothing

nothing

Done
Formal Semantics and Conservativeness

\[ T[G1] \iff GO \land S[G2] \]
Formal Semantics and Conservativeness

\[ T[G1] \iff GO \land S[G2] \]

\[ G1 \preceq G2 \implies S[G2] \rightarrow 0 \]
Weak Unemit Circuit