

Sequentiality and Determinacy for Reactive Systems

A Sequentially Constructive Circuit Semantics for Esterel

Alexander Schulz-Rosengarten,
Steven Smyth, Reinhard von Hanxleden, Kiel University
and Michael Mendler, Bamberg University

Berry Constructive Circuits (BCC)

```
module OffOn:  
  output S, T, U;  
  present S then emit T end;  
  emit S;  
  present S then emit U end
```

Berry Constructive Circuits (BCC)

```
module OffOn:  
  output S, T, U;  
  present S then emit T end;  
  emit S;  
  present S then emit U end
```

Constructive coherence law:

A signal is present/absent iff it must/cannot be emitted

Berry Constructive Circuits (BCC)

```
module OffOn:  
  output S, T, U;  
  present S then emit T end;  
  emit S;  
  present S then emit U end
```

Berry Constructive Circuits (BCC)

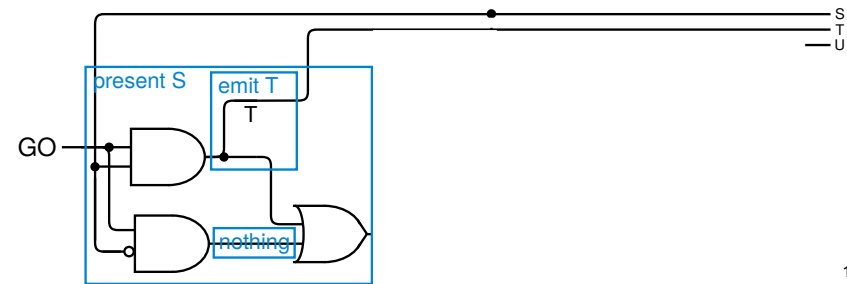
```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```

GO-

13

Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



15

Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```

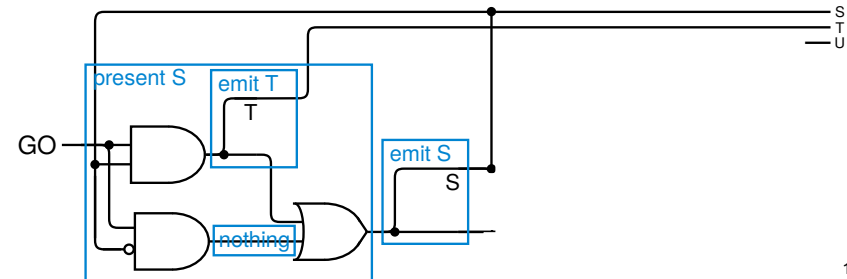
GO-

S
T
U

14

Berry Constructive Circuits (BCC)

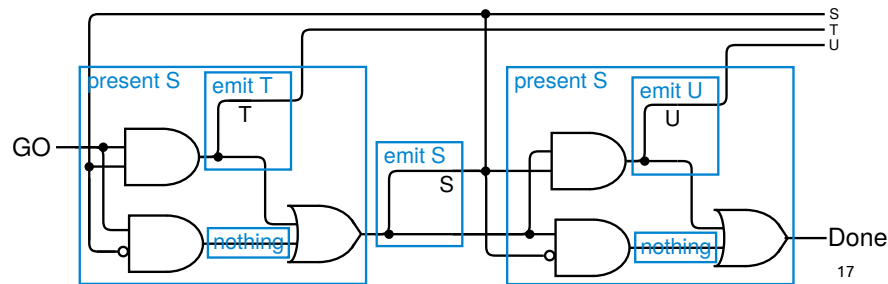
```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



16

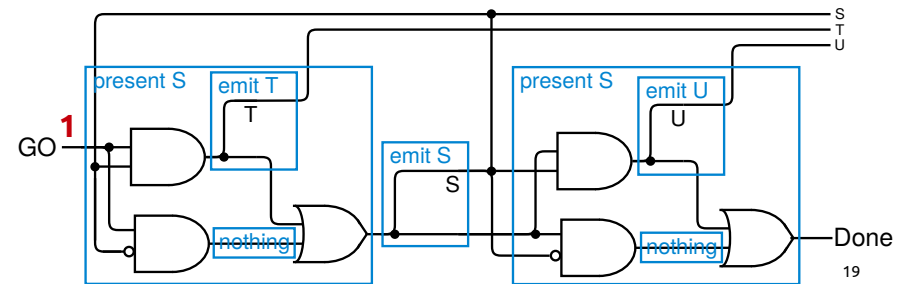
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



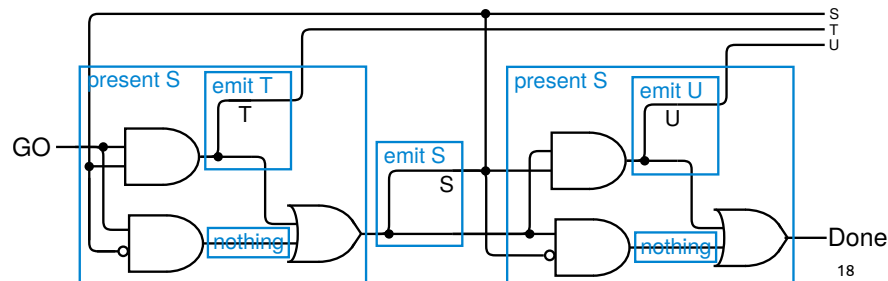
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



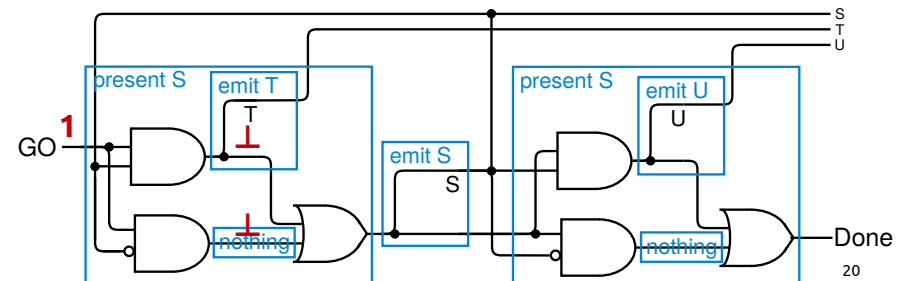
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



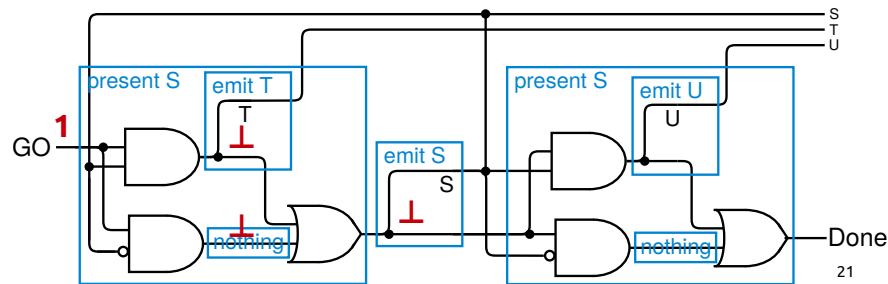
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



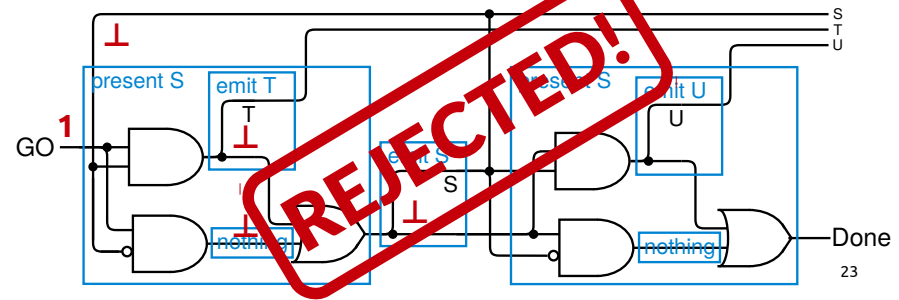
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



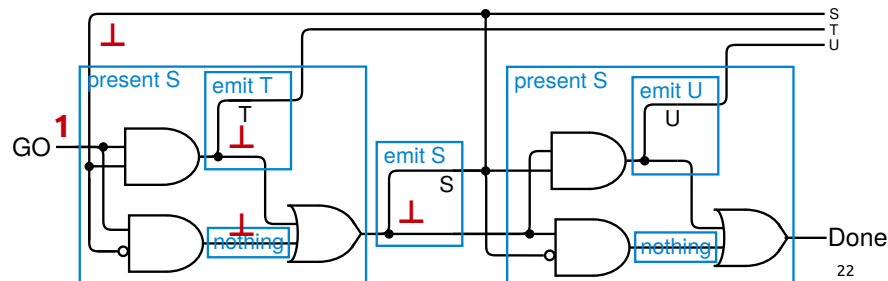
Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



Berry Constructive Circuits (BCC)

```
module Off0n:
output S, T, U;
present S then emit T end;
emit S;
present S then emit U end
```



Proposal

Recall:

Constructive coherence law:

A signal is present/absent iff it must/cannot be emitted

Proposal

Recall:

Constructive coherence law:

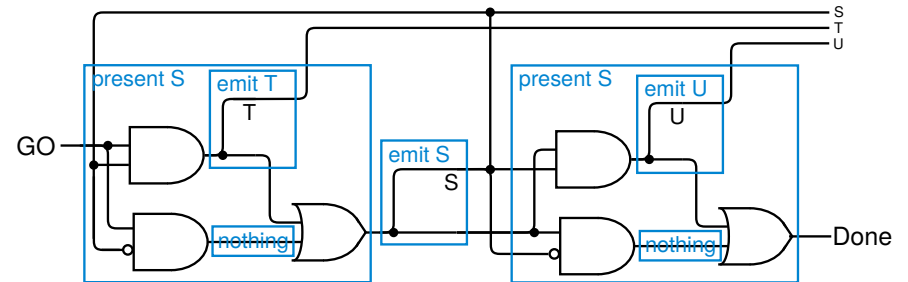
A signal is present/absent iff it must/cannot be emitted

Sequentially Constructive Coherence Law:

*A signal is present/absent iff it must/cannot be emitted
concurrently or sequentially preceding*

27

SC-Visibility in Circuits



29

Proposal

Recall:

Constructive coherence law:

A signal is present/absent iff it must/cannot be emitted

Sequentially Constructive Coherence Law:

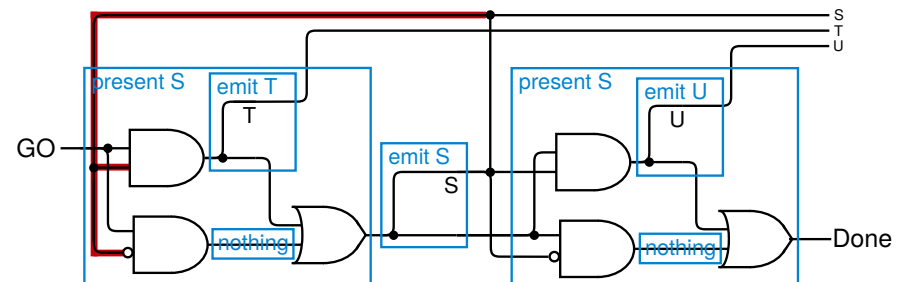
*A signal is present/absent iff it must/cannot be emitted
concurrently or sequentially preceding*

We say that an emit E is **SC-visible** to a present test P if:

- 1) E is concurrent to P or
- 2) E sequentially precedes P

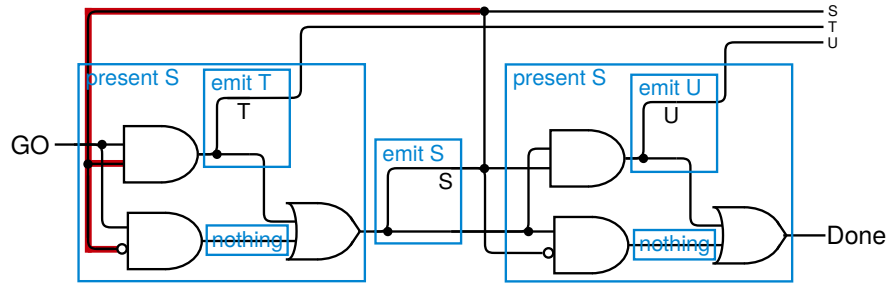
28

SC-Visibility in Circuits



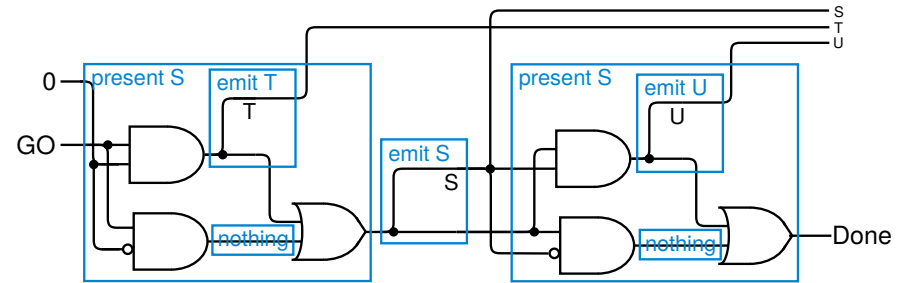
30

SC-Visibility in Circuits



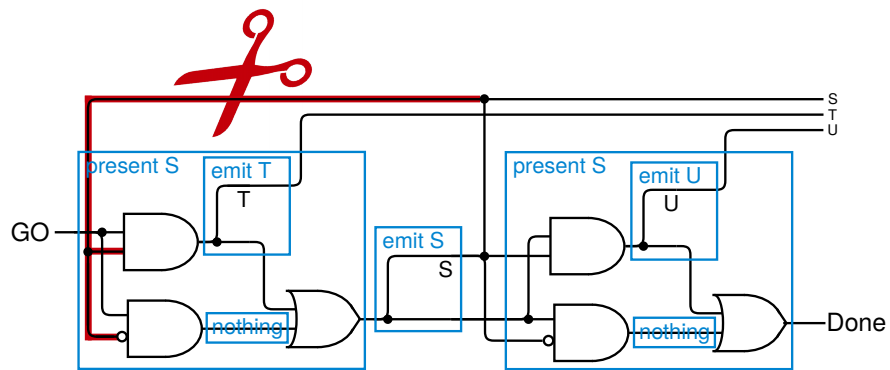
31

SC-Visibility in Circuits



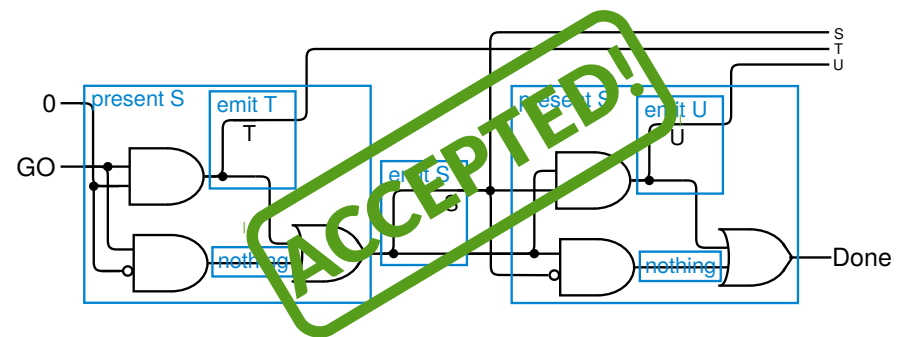
33

SC-Visibility in Circuits



32

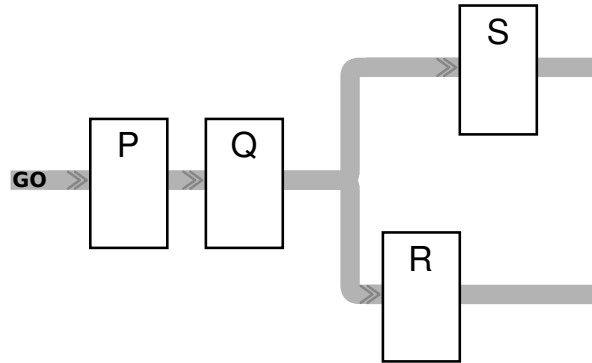
SC-Visibility in Circuits



34

SC-Visibility in Circuit Construction

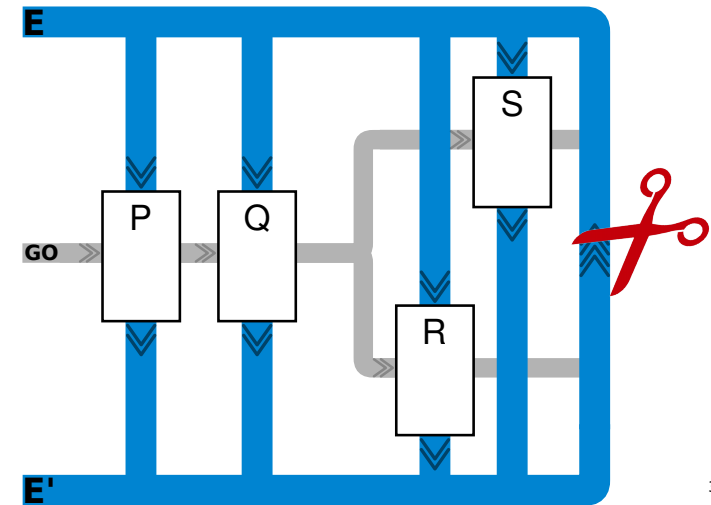
$P; Q; [R \parallel S]$



35

SC-Visibility in Circuit Construction

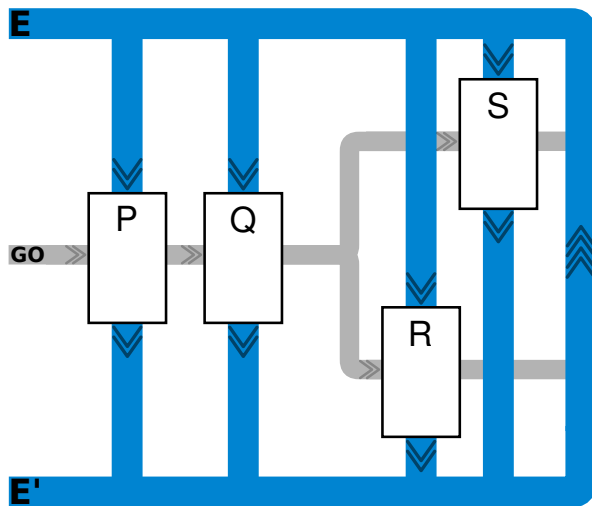
$P; Q; [R \parallel S]$



37

SC-Visibility in Circuit Construction

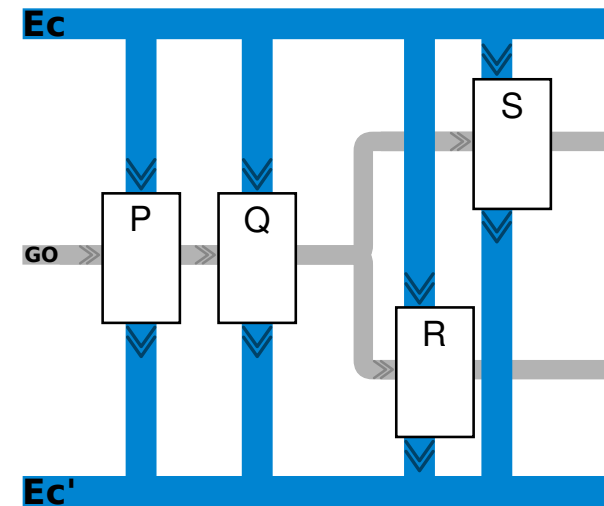
$P; Q; [R \parallel S]$



36

SC-Visibility in Circuit Construction

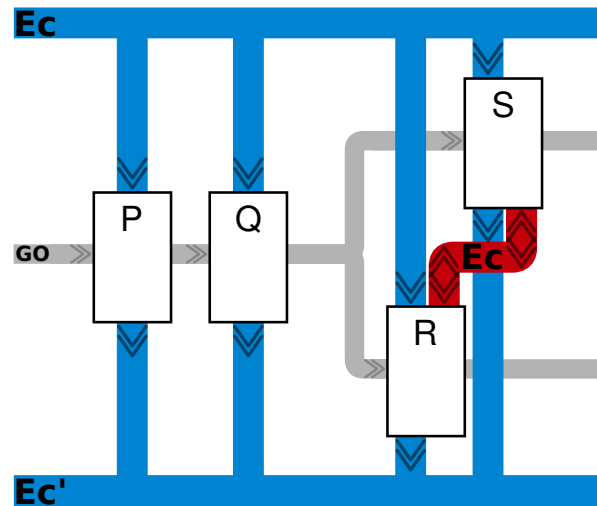
$P; Q; [R \parallel S]$



38

SC-Visibility in Circuit Construction

$P; Q; [R \parallel S]$



39

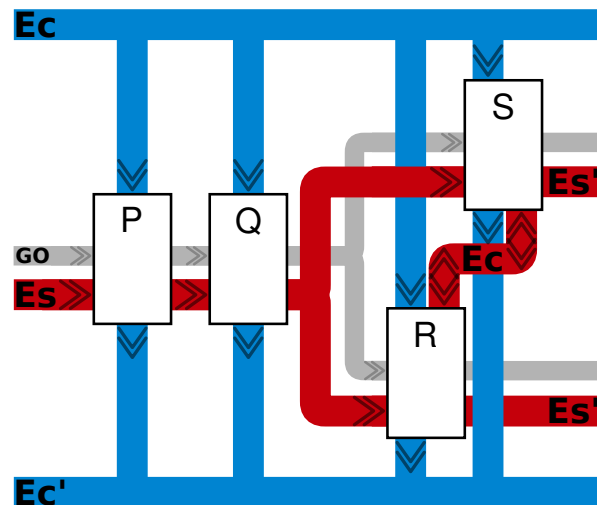
Circuit Interface

P	
E	E'
GO	SEL
RES	k0
SUS	k1
KILL	k2

41

SC-Visibility in Circuit Construction

$P; Q; [R \parallel S]$



40

Circuit Interface

P	
E	E'
GO	SEL
RES	k0
SUS	k1
KILL	k2

BCC
Berry Constructive
Circuit

42

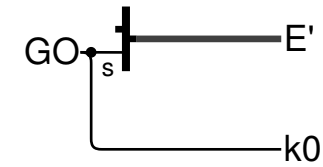
Circuit Interface



BCC
Berry Constructive
Circuit

43

emit s



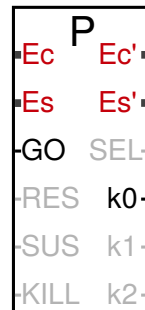
BCC

45

Circuit Interface



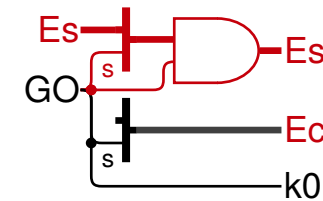
BCC
Berry Constructive
Circuit



SCC
Sequentially Constructive
Circuit

44

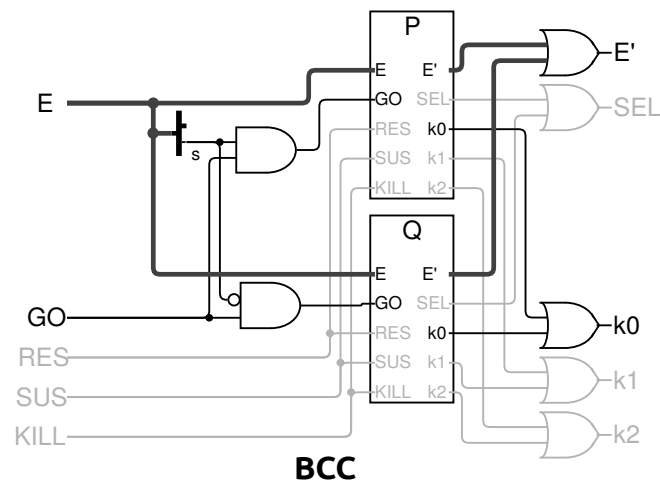
emit s



SCC

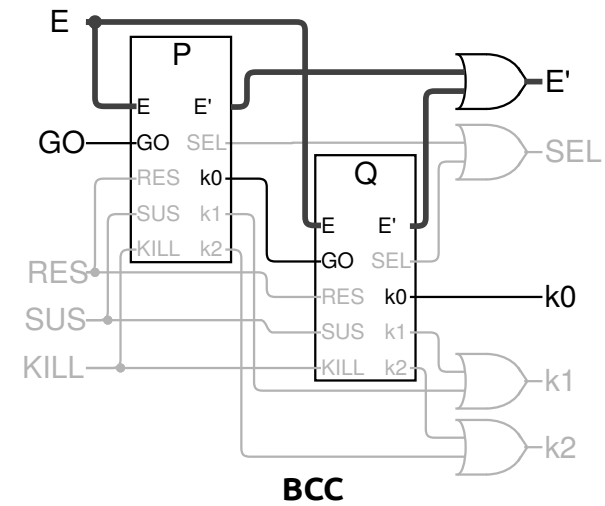
46

present s then P else Q



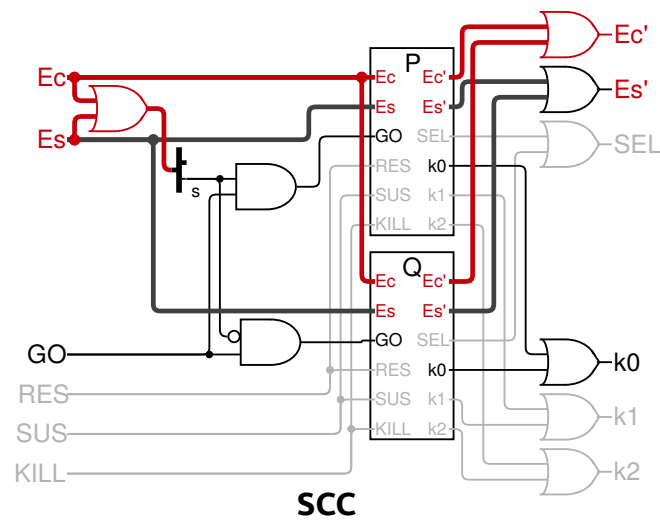
47

$P ; Q$



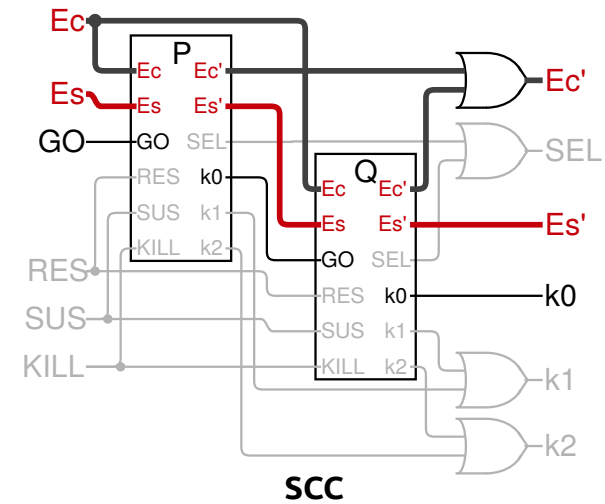
49

present s then P else Q



48

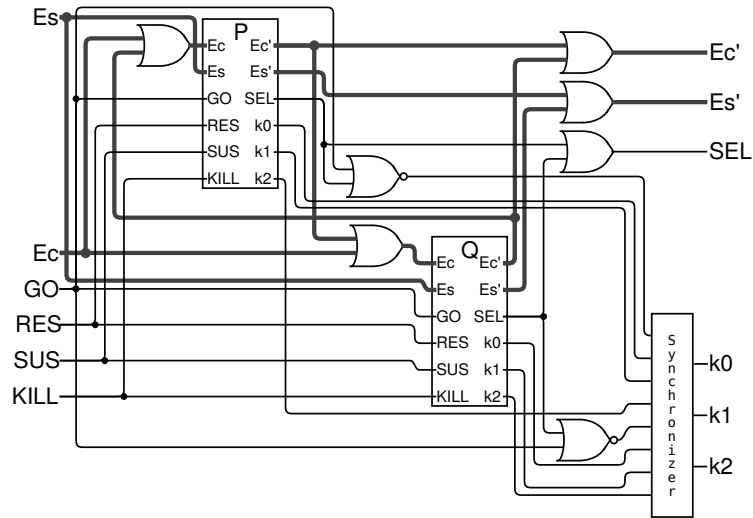
$P ; Q$



50

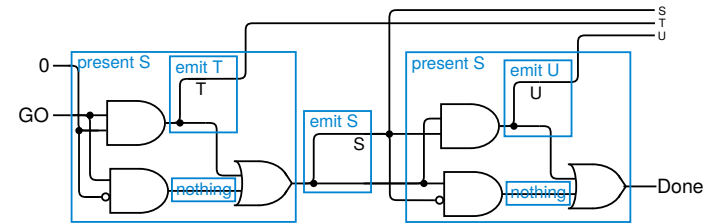
SCC Parallel

$P \parallel Q$



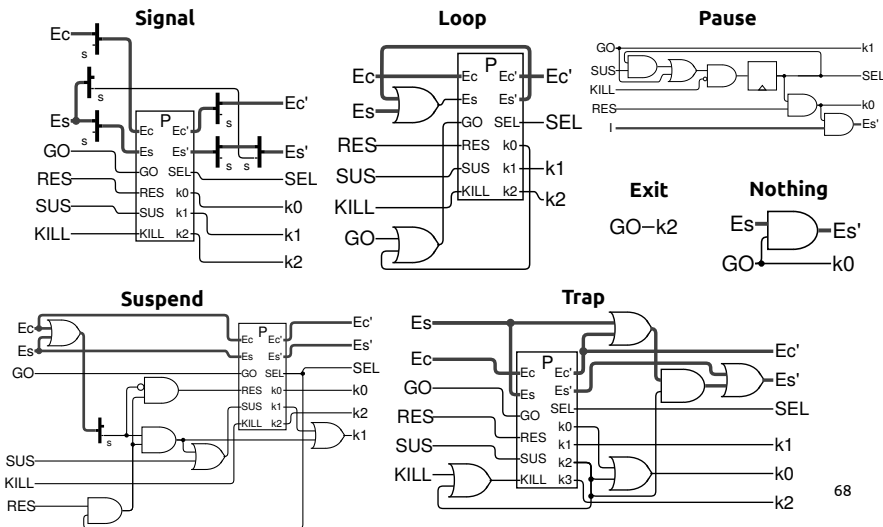
67

OffOn with SCC



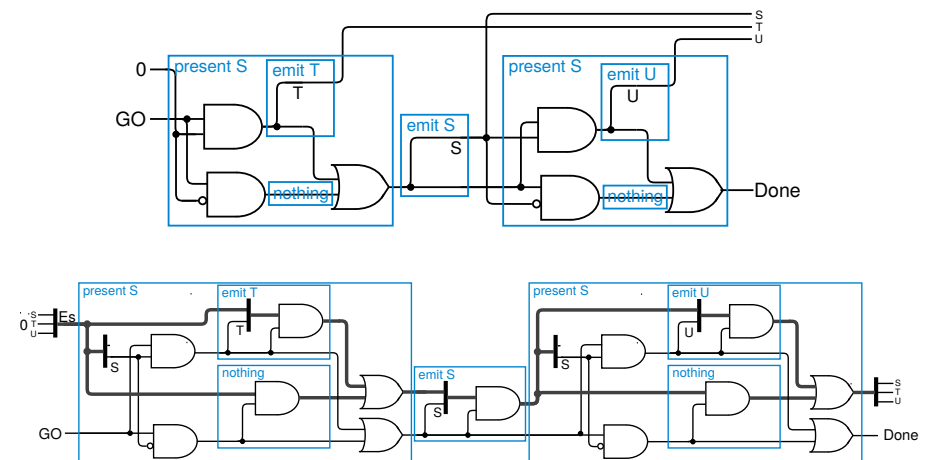
51

Further SCC Rules



68

OffOn with SCC



52

Formal Semantics and Conservativeness

Behavior of BC circuit with SC-visibility evaluation
 $\Rightarrow$ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801¹)

¹ A. Schulz-Rosengarten, S. Smyth, R. von Hanxleden, and M. Mendler, "A sequentially constructive circuit semantics for Esterel," Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1801, Feb. 2018, ISSN 2192-6247.

53

Formal Semantics and Conservativeness

Behavior of BC circuit with SC-visibility evaluation
 $\Rightarrow$ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801¹)

Evaluation Relation:

$$\mathcal{C}, I, R \vdash e \hookrightarrow_{\pi} b$$

Evaluation Rules:

$$\frac{\exists w \Leftarrow_l e \in \mathcal{C}. \pi \not\vdash l \wedge e \hookrightarrow_{\pi \oplus l} 1}{w \hookrightarrow_{\pi} 1} PRES(\pi, l)$$

$$\frac{\forall w \Leftarrow_l e \in \mathcal{C}. \pi \not\vdash l \Rightarrow e \hookrightarrow_{\pi \oplus l} 0}{w \hookrightarrow_{\pi} 0} ABS(\pi, w)$$

¹ A. Schulz-Rosengarten, S. Smyth, R. von Hanxleden, and M. Mendler, "A sequentially constructive circuit semantics for Esterel," Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1801, Feb. 2018, ISSN 2192-6247.

55

Formal Semantics and Conservativeness

Behavior of BC circuit with SC-visibility evaluation
 $\Rightarrow$ Behavior of SC circuit with BC evaluation
(Proof sketch in Technical Report 1801¹)

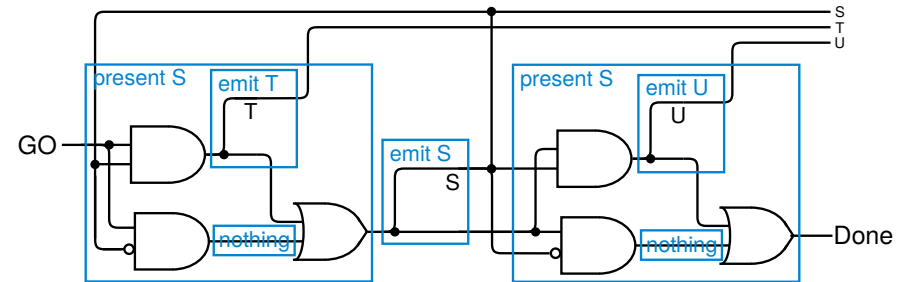
Evaluation Relation:

$$\mathcal{C}, I, R \vdash e \hookrightarrow_{\pi} b$$

¹ A. Schulz-Rosengarten, S. Smyth, R. von Hanxleden, and M. Mendler, "A sequentially constructive circuit semantics for Esterel," Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1801, Feb. 2018, ISSN 2192-6247.

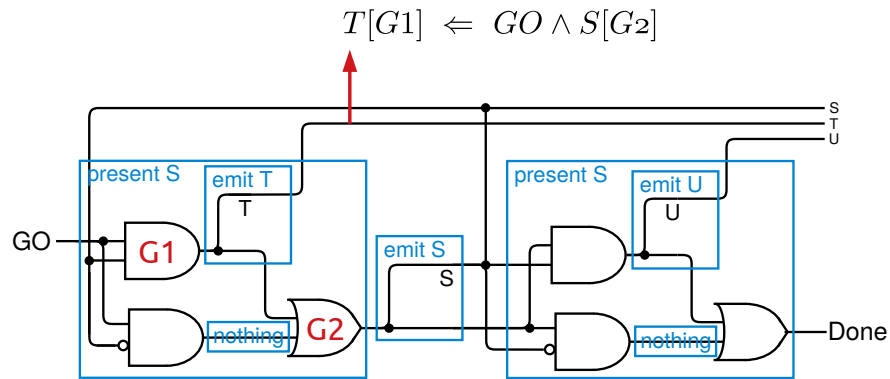
54

Formal Semantics and Conservativeness



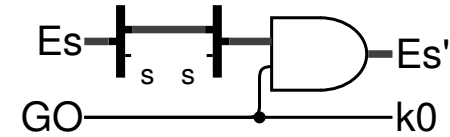
56

Formal Semantics and Conservativeness



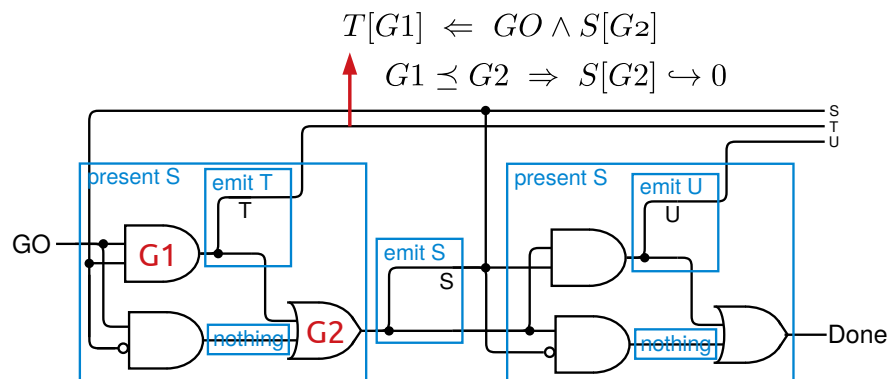
57

Weak Unemit Circuit



69

Formal Semantics and Conservativeness



58