Synchronous Languages—Lecture 13

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Sequentially Constructive Concurrency

The 5-Minute Review Session

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3. What is the *SCG*?
4. What are *basic blocks*? What are *scheduling blocks*?
5. When compiling from the SCG, what types of *low-level synthesis* do we distinguish? How do they compare?

Safety-Critical Embedded Systems

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- Computations often exploit *concurrency*
- Key challenge: **Concurrency must be deterministic!**

Thanks to Michael Mendler (U Bamberg) for support with these slides

Implementing (Deterministic) Concurrency

- **C, Java, etc.:**

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Aim: Deterministic concurrency with synchronous foundations, but without synchronous restrictions.

Comparing Both Worlds

Sequential Languages

- C, Java, ...

Synchronous Languages

- Esterel, Lustre, Signal, SCADE, SyncCharts ...

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  - Resolved by scheduler

Comparing Both Worlds (Cont'd)

Sequential Languages

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  - ☹ No guarantees of determinism or deadlock freedom

Synchronous Languages

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  - ☺ Deterministic concurrency and deadlock freedom

Comparing Both Worlds (Cont'd)

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  - ☹ No guarantees of determinism or deadlock freedom
  - ☺ Intuitive programming paradigm

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$$\Longrightarrow$$

Sequentially Constructive Model of Computation (SC MoC)

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☺ Intuitive programming paradigm

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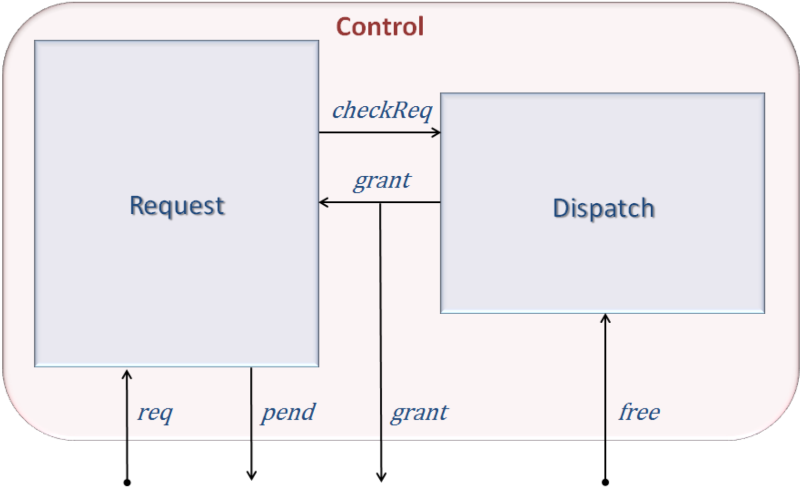
A Sequentially Constructive Program



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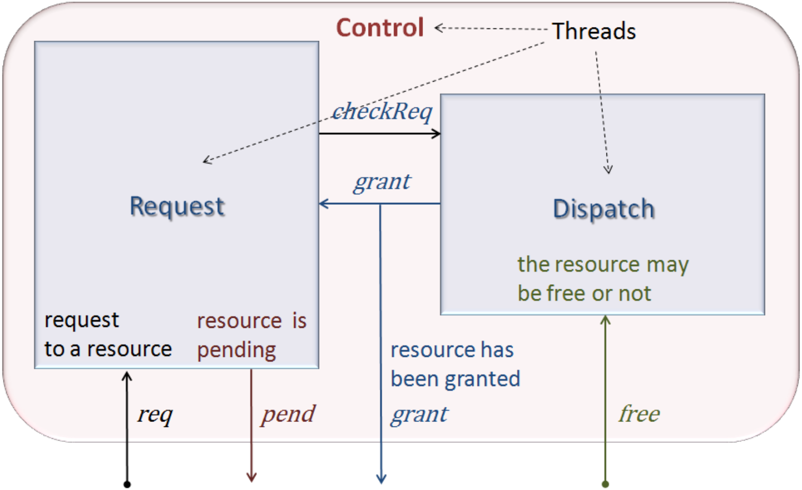

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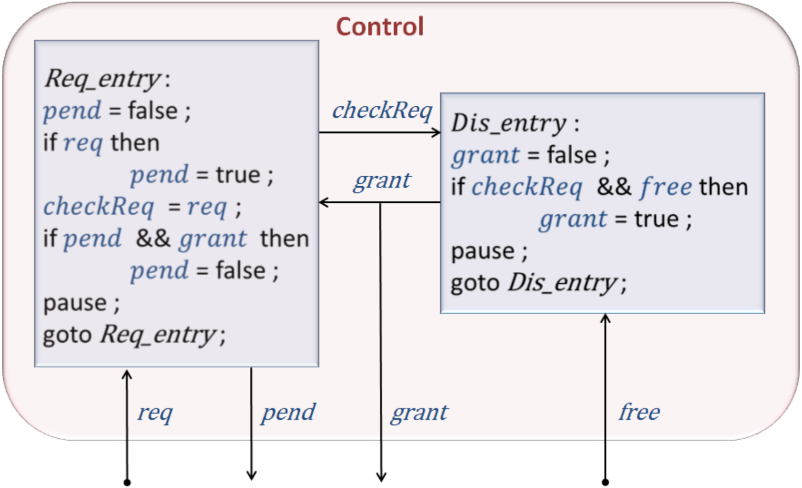

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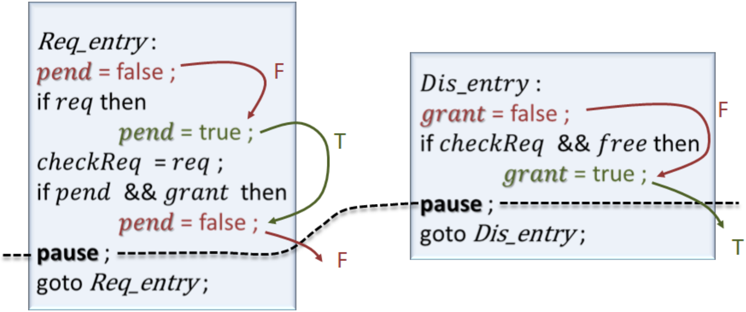

Imperative program order (sequential access to shared variables)

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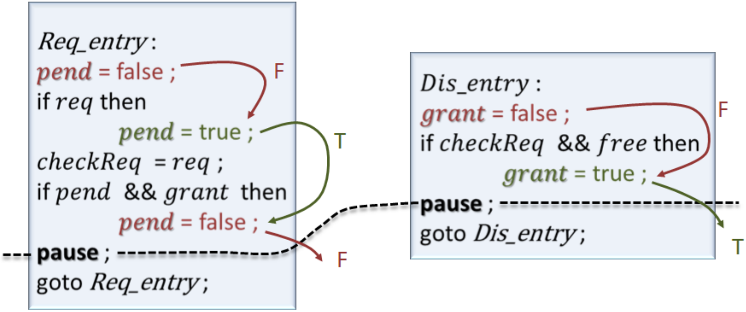

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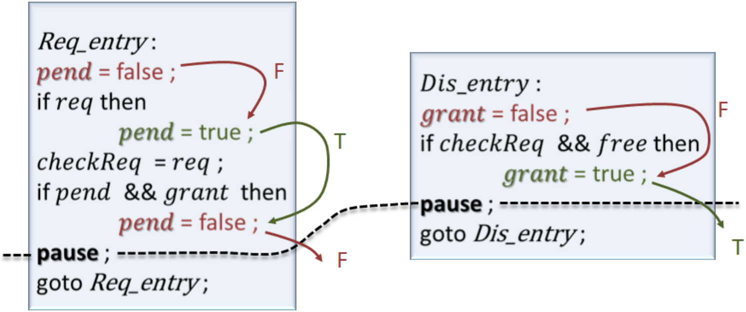

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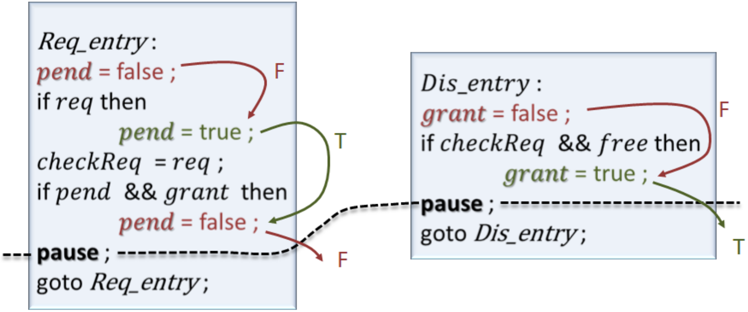

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  - ☺ Accepted in SC MoC
  - ☹ Not permitted in standard synchronous MoC

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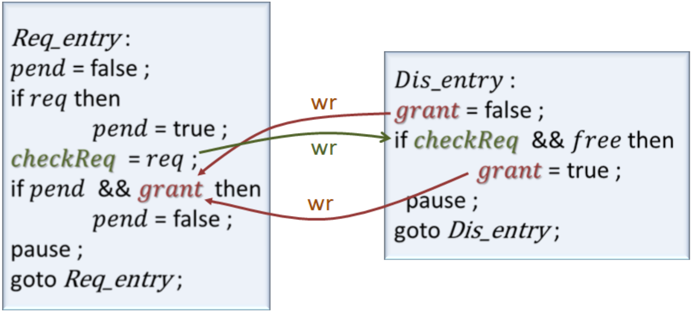

Concurrency scheduling constraints (access to shared variables):

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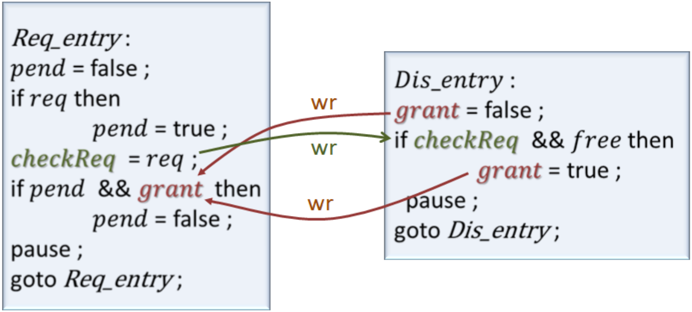

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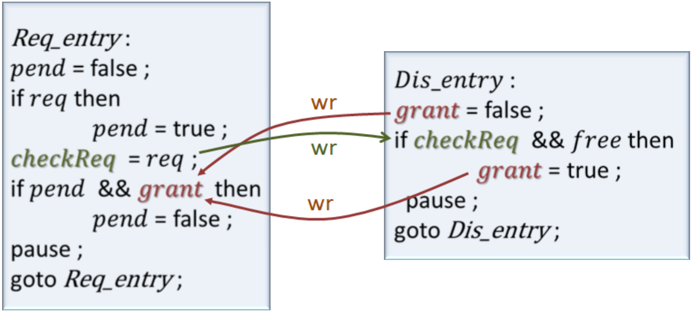

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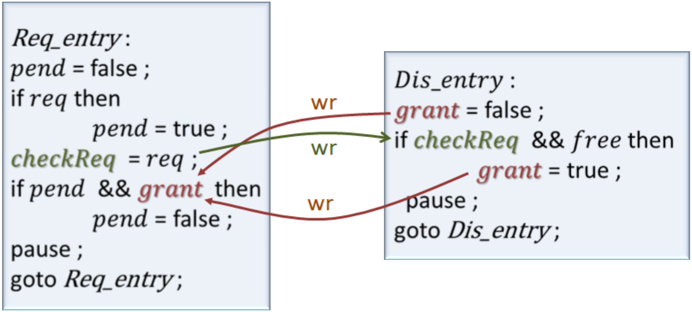

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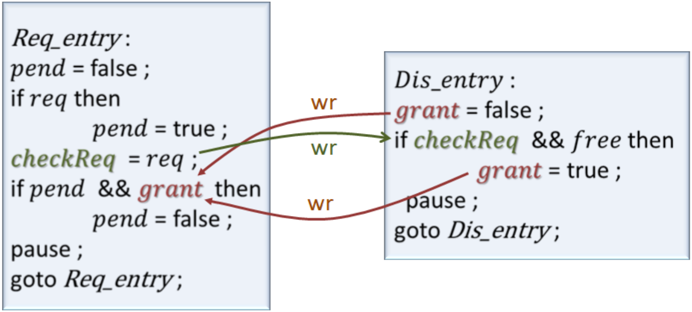

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- Implemented by the SC compiler

A Constructive Game of Schedulability

logically reactive program

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- Defines the rules
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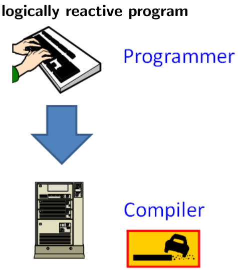

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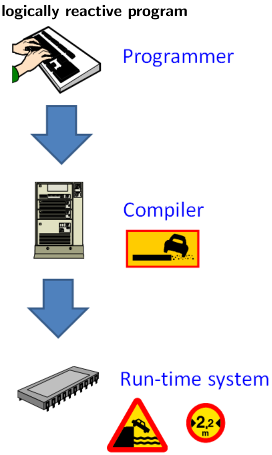

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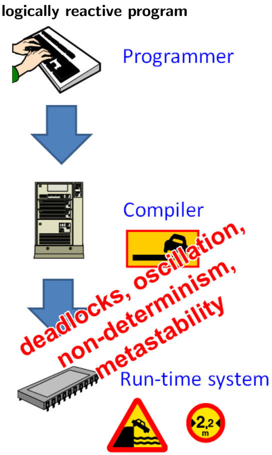

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The following applies to **concurrent** variable accesses only ...

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SC Concurrent Memory Access Protocol (per macro tick)

concurrent, multi-writer, multi-reader variables

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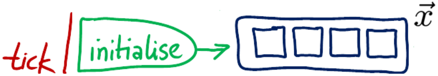

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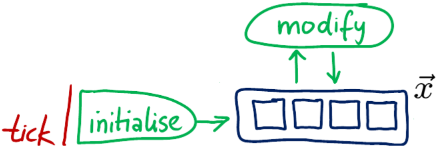

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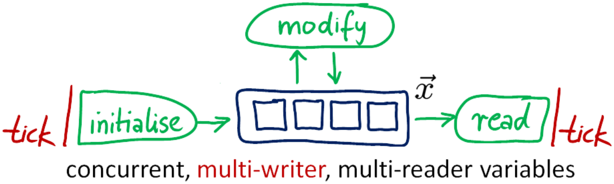

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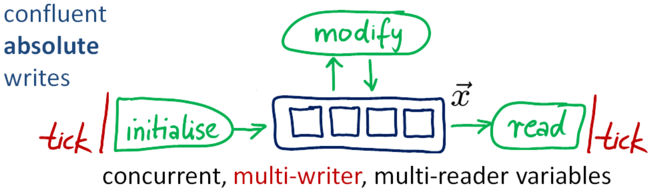

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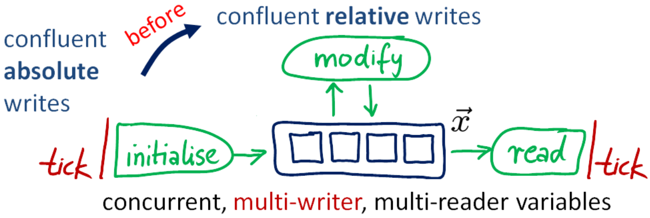

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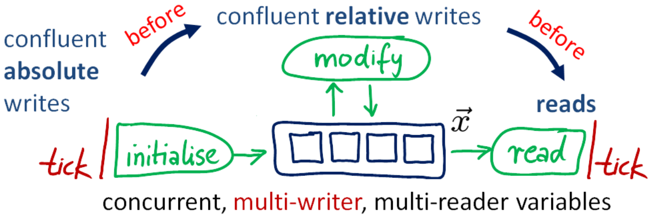

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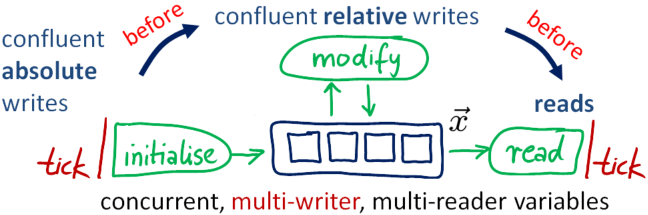

Confluent Statements (per macro tick)

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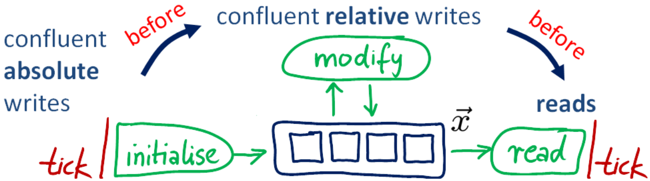

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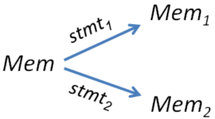

$stmt_1$, $stmt_2$ concurrent

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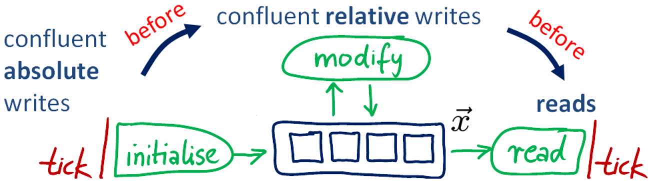

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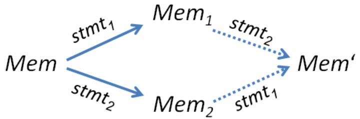

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Goals and Challenges

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3. Want to exploit sequentiality as much as possible
   - But what exactly *is* sequentiality?
4. Want to define not only the exact concept of SC, but also a practical strategy to implement it
   - In practice, this requires conservative approximations
   - Compiler must not accept Non-SC programs
   - Compiler may reject SC programs

References

Most of the material here draws from this reference [TECS]:

R. von Hanxleden, M. Mendler, J. Aguado, B. Duderstadt, I. Fuhrmann, C. Motika, S. Mercer, O. O'Brien, and P. Roop.
Sequentially Constructive Concurrency – A Conservative Extension of the Synchronous Model of Computation.
ACM Transactions on Embedded Computing Systems, Special Issue on Applications of Concurrency to System Design, July 2014, 13(4s).
https://rtsys.informatik.uni-kiel.de/~biblio/downloads/papers/tecs14.pdf

Unless otherwise noted, the numberings of definitions, sections etc. refer to this.

There is also an extended version [TR]:

R. von Hanxleden, M. Mendler, J. Aguado, B. Duderstadt, I. Fuhrmann, C. Motika, S. Mercer, O. O'Brien, and P. Roop.
Sequentially Constructive Concurrency – A Conservative Extension of the Synchronous Model of Computation.
Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1308, ISSN 2192-6247, Aug. 2013, 13(4s).
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Overview

The Sequentially Constructive Language (SCL) [Sec. 2.1]

- Foundation for the SC MoC

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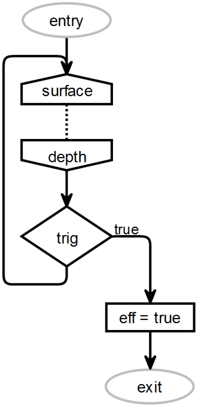
$$s ::= \quad x = e \mid s;s \mid \textbf{if } (e)\ s \textbf{ else } s \mid l \textbf{ : } s \mid \textbf{goto } l \mid \textbf{fork } s \textbf{ par } s \textbf{ join} \mid \textbf{pause}$$

s Statement
x Variable
e Expression
l Program label

The SC Graph (SCG) [Sec. 2.3]



The concurrent and sequential control flow of an SCL program is given by an SC Graph (SCG)

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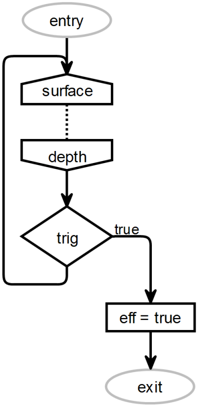

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Internal representation for

- Semantic foundation
- Analysis
- Code generation

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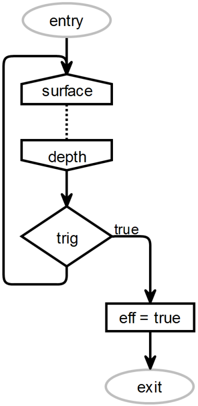

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SC Graph:

Labeled graph $G = (N, E)$

- Nodes N correspond to statements of sequential program
- Edges E reflect sequential execution control flow

Node Types in the SCG

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- $n.st \in$ $\{\text{entry, exit, goto, } x = ex\text{, if}\,(ex)\text{, fork, join, surf, depth}\}$
- x: variable, ex: expression.

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- flow edges $\alpha_{flow} =_{\text{def}} \{seq, tick\}$

Edge Types in the SCG [Def. 2.1]

Edge $e \in E$ has edge type $e.type \in \alpha_a$

- Specifies the nature of the particular ordering constraint expressed by e
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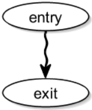
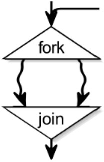
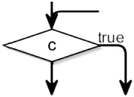
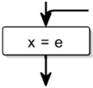
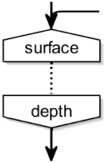
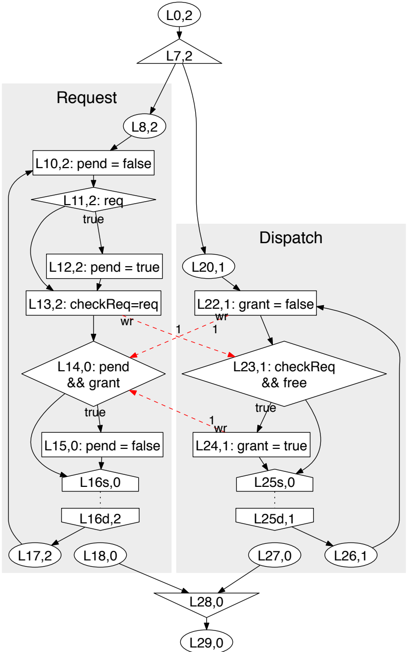
Mapping SCL & SCG

	Thread (Region)	Concurrency (Superstate)	Conditional (Trigger)	Assignment (Effect)	Delay (State)
SCG					
SCL	t	fork t_1 par t_2 join	if (c) s_1 else s_2	$x = e$	pause

Plus ";" (Sequence) and "goto" to specify sequential successors (solid edges)

SCL & SCG – The Control Example

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- Each $n \in N$ belongs to a thread $th(n)$ defined as
  - Immediately enclosing thread $t \in T$
  - such that there is a flow path to n that originates in t_{en}, *does not traverse* t_{ex},[1]

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- For each thread t, define $sts(t)$ as the set of statement nodes $n \in N$ such that $th(n) = t$

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    if (req)
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      pend = false;
    pause;
    goto Request entry;
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    pause;
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  }
  join;
}
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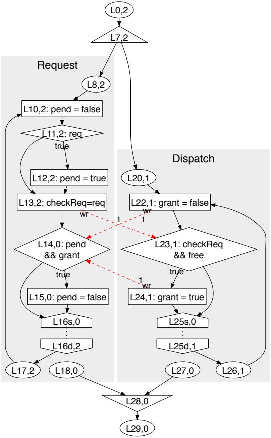

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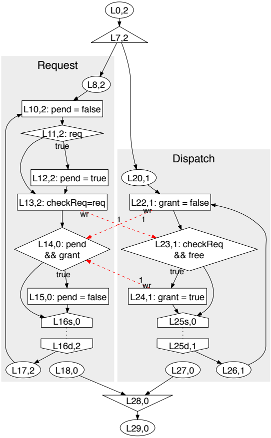

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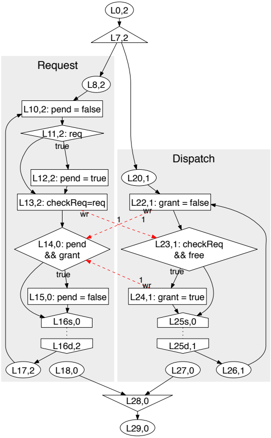

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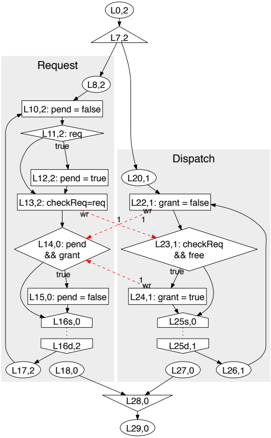

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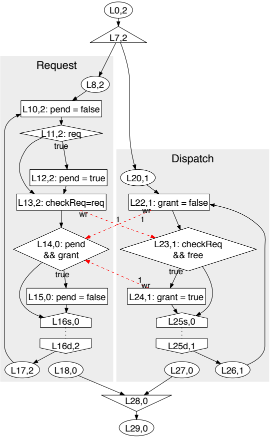

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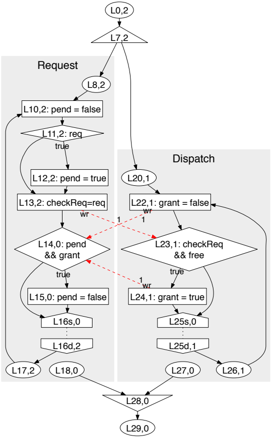

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- *Root* thread consists of the statement nodes $sts(Root) = \{L0, L7, L28, L29\}$
- The remaining statement nodes of N are partitioned into $sts(Dispatch)$ and $sts(Request)$

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Let t, t_1, t_2 be threads in T

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- t_1 is subordinate to t_2, written $t_1 \prec t_2$, if $t_1 \neq t_2 \wedge t_1 \in p^*(t_2)$
- t_1 and t_2 are (statically) concurrent, denoted $t_1 \,||\, t_2$, iff t_1 and t_2 are descendants of distinct threads sharing a common fork node, *i. e.*:

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  $p(t) =_{def} th(fork(t))$, the parent thread
- $p^*(t) =_{def} \{t, p(t), p(p(t)), \ldots, \text{Root}\}$, the recursively defined set of ancestor threads of t
- t_1 is subordinate to t_2, written $t_1 \prec t_2$, if $t_1 \neq t_2 \wedge t_1 \in p^*(t_2)$
- t_1 and t_2 are (statically) concurrent, denoted $t_1 \,||\, t_2$, iff t_1 and t_2 are descendants of distinct threads sharing a common fork node, *i. e.*:
  $\exists t_1' \in p^*(t_1), t_2' \in p^*(t_2) : \; t_1' \neq t_2' \wedge fork(t_1') = fork(t_2')$

Static Thread Concurrency and Subordination [Def. 2.2]

Let t, t_1, t_2 be threads in T

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  - Denote this common fork node as $lcafork(t_1, t_2)$, the least common ancestor fork

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Let t, t_1, t_2 be threads in T

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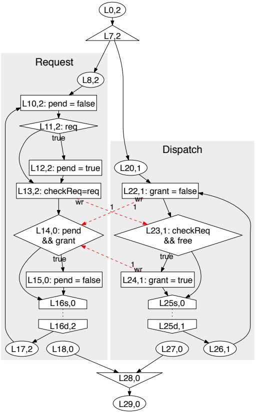
  - Denote this common fork node as $\mathit{lcafork}(t_1, t_2)$, the least common ancestor fork
  - Lift (static) concurrency notion to nodes: $n_1 \,||\, n_2 \Leftrightarrow \mathit{th}(n_1) \,||\, \mathit{th}(n_2) \Leftrightarrow \mathit{lcafork}(n_1, n_2) = \mathit{lcafork}(\mathit{th}(n_1), \mathit{th}(n_2))$

Concurrency and Subordination in Control-Program

```
module Control
input bool free, req;
output bool grant, pend;
{
  bool checkReq;

  fork {
    // Thread Request
    Request entry:
    pend = false;
    if (req)
      pend = true;
    checkReq = req;
    if (pend && grant)
      pend = false;
    pause;
    goto Request entry;
  }
  par {
    // Thread Dispatch
    Dispatch entry:
    grant = false;
    if (checkReq && free)
      grant = true;
    pause;
    goto Dispatch entry;
  }
  join;
}
```



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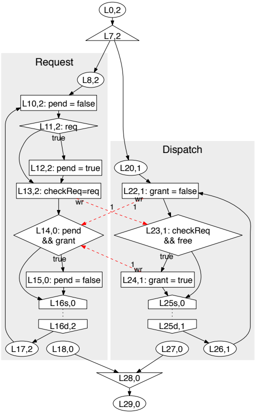

- *Root* $\prec$ *Request* and *Root* $\prec$ *Dispatch*

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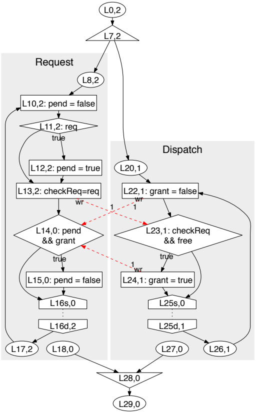

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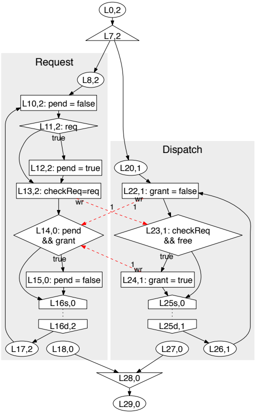

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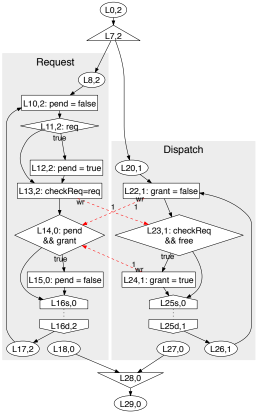

- *Root* $\prec$ *Request* and *Root* $\prec$ *Dispatch*
- *Request* $||$ *Dispatch*, *Root* is not concurrent with any thread

Note: Concurrency on threads, in contrast to concurrency on node instances, is purely static and can be checked with a simple, syntactic analysis of the program structure.

Thread Trees [TR, Sec. 3.7]

A Thread Tree illustrates the static thread relationships.

- Contains subset of SCG nodes:
  1. Entry nodes, labeled with names of their threads
  2. Fork nodes, attached to the entry nodes of their threads
- Similar to the AND/OR tree of Statecharts

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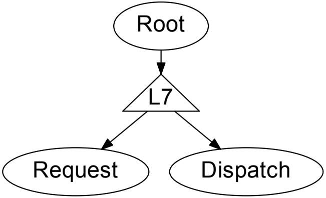

Thread Trees – The Reinc2 Example

```
module Reinc2
output int x, y;
{
 loop:
  fork { // Thread T1
    x = 1; }
  par { // Thread T2
    fork { // Thread T21
      y = 1; }
    par { // Thread T22
      pause;
      y = 2; }
    join;
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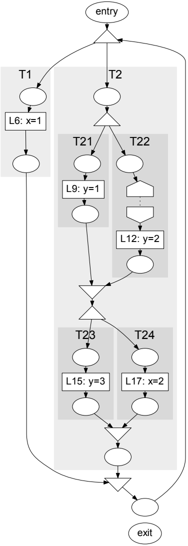

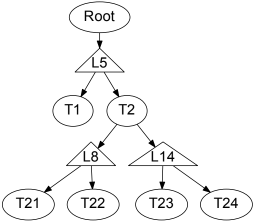

Alternative definition for static thread concurrency:

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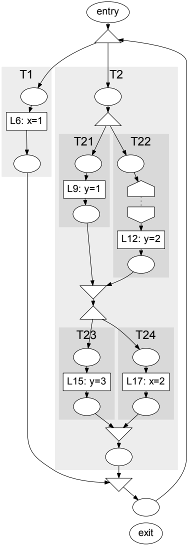

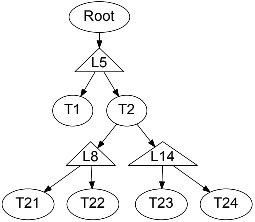

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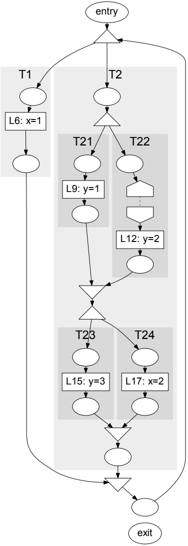

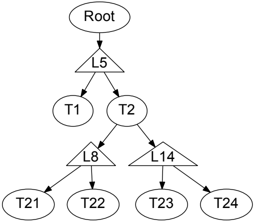

Alternative definition for static thread concurrency:

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Thread Reincarnation – The Reinc Example

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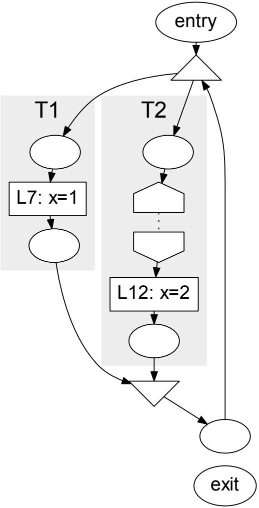

Are interested in run-time concurrency, *i. e.*, whether ordering is up to discretion of a scheduler.

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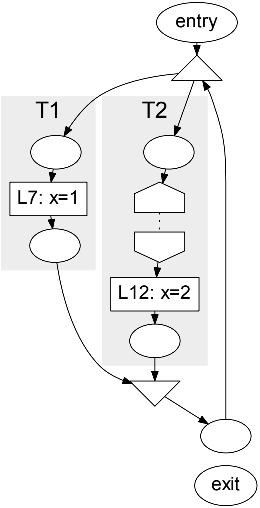

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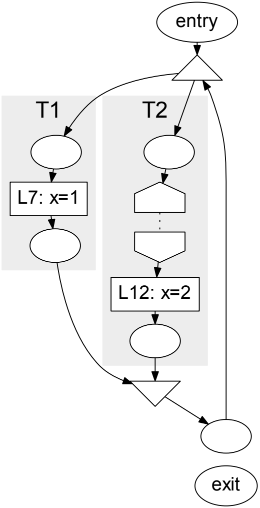

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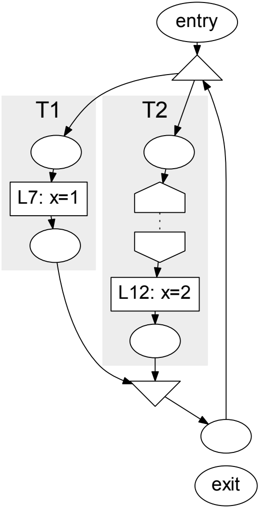

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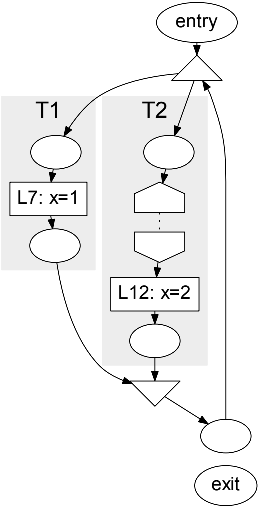
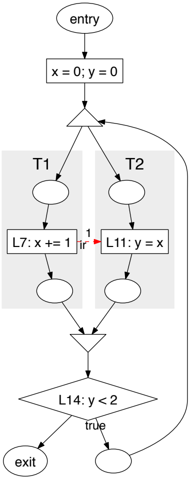


Are interested in run-time concurrency, *i. e.*, whether ordering is up to discretion of a scheduler.

Observations:

- T2 exhibits thread reincarnation
- Assignments to *x* are both executed in the same tick, yet are sequentialized
- Thus, **static thread concurrency not sufficient to capture run-time concurrency**!

Statement Reincarnation I

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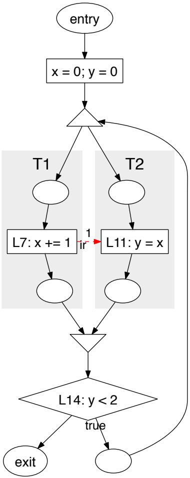


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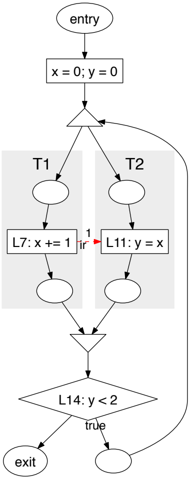


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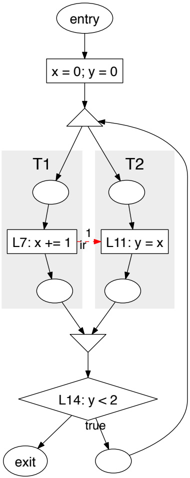


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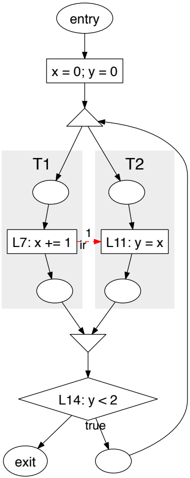


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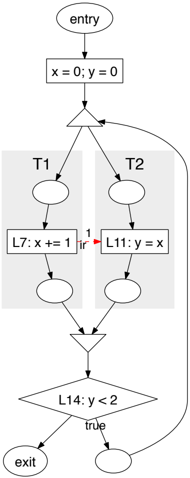


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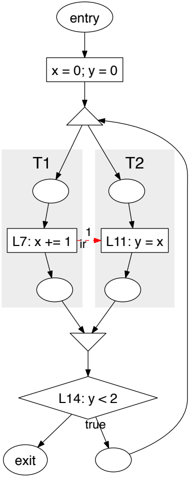
Not enough to impose an order on the program statements
$\Rightarrow$ Need to distinguish statement instances

Statement Reincarnation II

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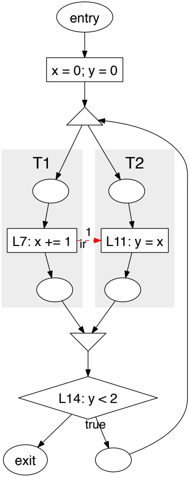


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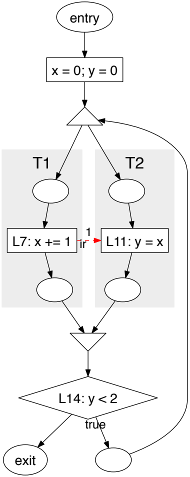


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- *Instantaneous loops* traditionally forbidden

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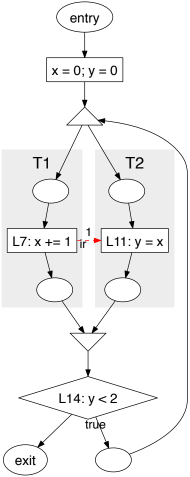


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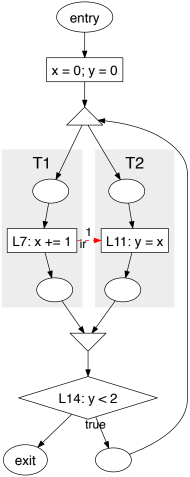
  - *Instantaneous loops* traditionally forbidden
- ☺ SC: Determinate ⇒ Accept

Statement Reincarnation II




```
module InstLoop
output int x = 0, y = 0;
{
loop:
 fork {
  // Thread T1
  x += 1;
 }
 par {
  // Thread T2
  y = x;
 }
 join;
 if (y < 2)
  goto loop;
}
```

- ☹ Traditional synchronous languages: Reject
  - *Instantaneous loops* traditionally forbidden
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  - One might still want to ensure that a program **always terminates**

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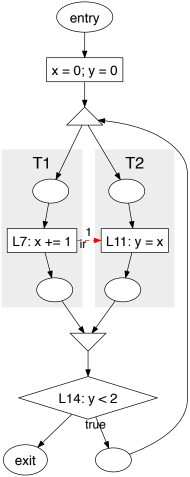


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- One might still want to ensure that a program **always terminates**
- But this issue is **orthogonal to determinacy** and having a well-defined semantics.

Macroticks [Def. 2.3 + 2.4]

- Given: SCG $G = (N, E)$
- (Macro) tick R, of length $len(R) \in \mathbb{N}_{\geq 1}$:
  mapping from micro tick indices $1 \leq j \leq len(R)$,
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- Node instance: $ni = (n, i)$,
  with statement node $n \in N$,
  micro tick count $i \in \mathbb{N}$
- Can identify macro tick R with set
  $\{(n, i) \mid 1 \leq i \leq len(R), n = R(i)\}$

Run-Time Concurrency [Def. 2.5 + 2.6]

Given: macro tick R, index $1 \leq i \leq len(R)$, node $n \in N$

Def.: $last(n, i) = max\{j \mid j \leq i, R(j) = n\}$,

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2. they belong to statically concurrent threads, *i. e.*, $th(n_1) \mid\mid th(n_2)$, and
3. their threads have been instantiated by the same instance of the associated least common ancestor fork, *i. e.*, $last(n, i_1) = last(n, i_2)$ where $n = lcafork(n_1, n_2)$

Overview

Continuations & Thread Execution States [Def. 3.1]

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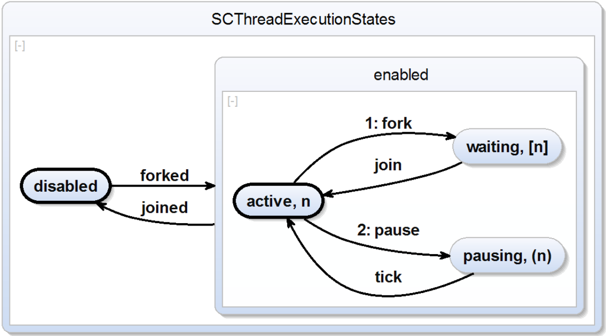

In a trace (see later slide), round/square/no parentheses around $n = c.node$ denote $c.status$, for enabled continuations c

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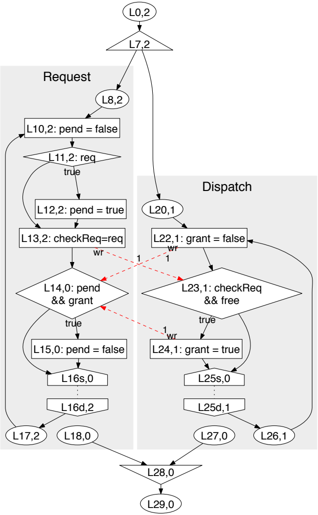
A configuration is called valid if C is valid

```
module Control
input bool free, req;
output bool grant, pend;
{
  bool checkReq;

  fork {
    // Thread Request
    Request entry:
    pend = false;
    if (req)
      pend = true;
    checkReq = req;
    if (pend && grant)
      pend = false;
    pause;
    goto Request entry;
  }
  par {
    // Thread Dispatch
    Dispatch entry:
    grant = false;
    if (checkReq && free)
      grant = true;
    pause;
    goto Dispatch entry;
  }
  join;
}
```



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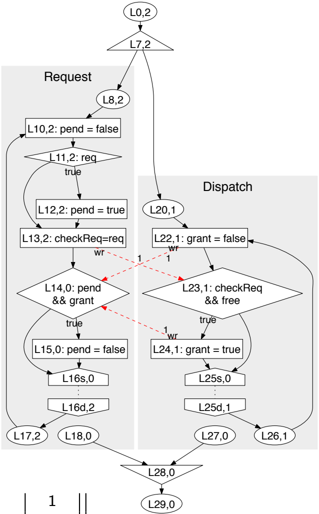

Macro tick	*a*	1												1
Micro tick	*i*	1	2	3	4	5	6	7	8	9	10	11	12	12
Input	free	**t**												*t*
vars	req	**f**												*f*
Output	grant	⊥								*f*				**f**
vars	pend	⊥				*f*								**f**
Local var	checkReq	⊥						*f*						*f*
	C_{Root}	L0	L7	[L28]										[L28]
Continuations	$C_{Request}$	⊥		L8	L10	L11	L13	L14	L14	L14	L14	L14	L16s	(L16s)
	$C_{Dispatch}$	⊥		L20	L20	L20	L20	L20	L22	L23	L25s	(L25s)	(L25s)	(L25s)
Scheduled nodes R_i^a		L0	L7	L8	L10	L11	L13	L20	L22	L23	L25s	L14	L16s	

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3  output bool grant, pend;
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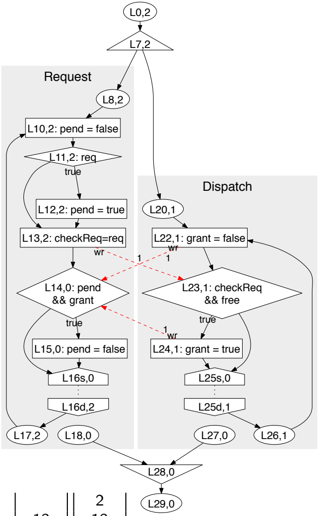

Macro tick	*a*	2													2
Micro tick	*i*	1	2	3	4	5	6	7	8	9	10	11	12	13	13
Input	free	**t**													*t*
vars	req	**t**													*t*
Output	grant	*f*							*f*		*t*				**t**
vars	pend	*f*		*f*		*t*								*f*	**f**
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Now define free scheduling, to set the stage for later defining "initialize-update-read" protocol
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2. Do so in an interleaving fashion

Micro Steps I

Micro step: transition $(C_{cur}, M_{cur}) \xrightarrow{c}_{\mu s} (C_{nxt}, M_{nxt})$ between two micro ticks

- (C_{cur}, M_{cur}): current configuration
- c: continuation selected for execution
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The free schedule is permitted to pick any one of the $\prec$-maximal continuations $c \in C_{cur}$ with $c.status =$ active and execute it in the current memory M_{cur}

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- Actions μM and μC (made precise in paper) depend on the statement $c.node.st$ to be executed
- (C_{nxt}, M_{nxt}) uniquely determined by c, thus may write $(C_{nxt}, M_{nxt}) = c(C_{cur}, M_{cur})$

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Otherwise:

- Scheduler can perform a global clock step

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- Transition between last micro tick of the current macro tick to first micro tick of the subsequent macro tick
- All pausing continuations of C advance from their surf node to the associated depth node:

$$C_{nxt} = \{c[\text{active} :: tick(n)] \mid c[\text{pausing} :: n] \in C_{cur}\} \cup \{c[\text{waiting} :: n] \mid c[\text{waiting} :: n] \in C_{cur}\}$$

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Formally,

$$M_{nxt}(x) = \begin{cases} v_i, & \text{if } x = x_i \in I, \\ M_{cur}(x), & \text{if } x \notin I. \end{cases}$$

Macro Ticks

Scheduler runs through sequence

$$(C_0^a, M_0^a) \xrightarrow{c_1^a}_{\mu s} (C_1^a, M_1^a) \xrightarrow{c_2^a}_{\mu s} \cdots \xrightarrow{c_{k(a)}^a}_{\mu s} (C_{k(a)}^a, M_{k(a)}^a) \tag{1}$$

to reach final quiescent configuration $(C_{k(a)}^a, M_{k(a)}^a)$

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Sequence (1) is macro tick (synchronous instant) a:

$$(R^a, V_I^a) : (C_0^a, M_0^a) \Longrightarrow (C_{k(a)}^a, M_{k(a)}^a) \qquad (2)$$

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R^a: sequence of statement nodes executed during a

- $len(R^a) = k(a)$ is length of a
- R^a is function mapping each micro tick index $1 \leq j \leq k(a)$ to node $R^a(j) = c_j^a.node$ executed at index j

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- all macro tick configurations are connected by clock steps, i.e., $(C_{k(a)}^a, M_{k(a)}^a) \rightarrow_{tick} (C_0^{a+1}, M_0^{a+1})$

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Run of G: sequence of macro ticks R^a and external inputs V_I^a, with

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- all macro tick configurations are connected by clock steps, i.e., $(C^a_{k(a)}, M^a_{k(a)}) \rightarrow_{tick} (C_0^{a+1}, M_0^{a+1})$

Trace: externally visible output values at each macro tick R [TR, Sec. 3.9]

Determinacy

Recall:

$$(C_0^a, M_0^a) \xrightarrow{c_1^a}_{\mu s} (C_1^a, M_1^a) \xrightarrow{c_2^a}_{\mu s} \cdots \xrightarrow{c_{k(a)}^a}_{\mu s} (C_{k(a)}^a, M_{k(a)}^a) \qquad (1)$$

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- only macro configurations are observable externally (in fact, only the memory component of those)
- **Suffices to ensure that sequence of macro ticks $\Longrightarrow$ is determinate**
- Micro tick behavior $\rightarrow_{\mu s}$ may well be non-determinate

Active and Pausing Continuations are Concurrent [TR, Prop. 2]

Given:

- (C, M), reachable (micro or macro tick) configuration
- $c_1, c_2 \in C$, active or pausing continuations with $c_1 \neq c_2$

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Then:

- $c_1.node \neq c_2.node$
- $th(c_1.node) \,||\, th(c_2.node)$
- No instantaneous sequential path from $c_1.node$ to $c_2.node$ or vice versa

(Proof: see [TR])

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Recall: Want to exploit sequentiality as much as possible

- Thus, consider only run-time concurrent data dependencies

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- Thus, consider only run-time concurrent data dependencies

Recall: Static concurrency $\not\Rightarrow$ run-time concurrency

- Consider Reinc example
- Thus, can ignore some statically concurrent data dependencies

Concurrency vs. Sequentiality Revisited II

Question: Does (static) sequentiality preclude run-time concurrency?

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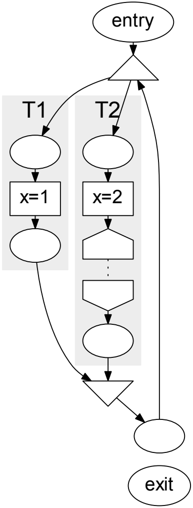

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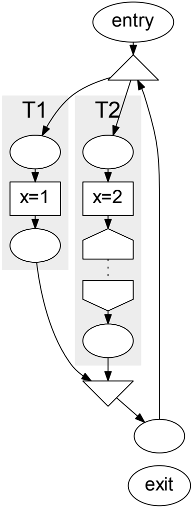

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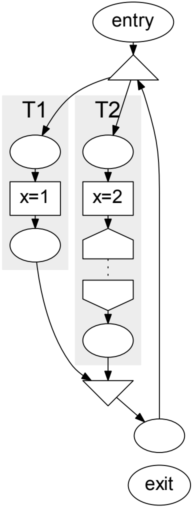

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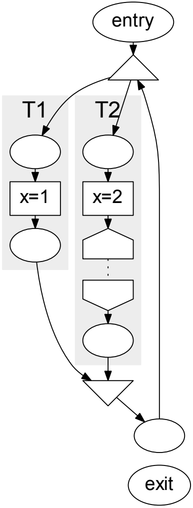

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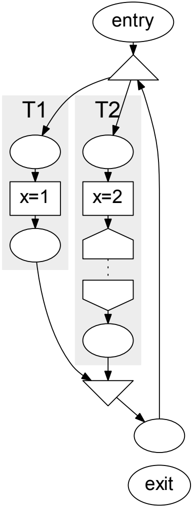
Thus, concurrency and (static) sequentiality are not **mutually exclusive, but orthogonal**!



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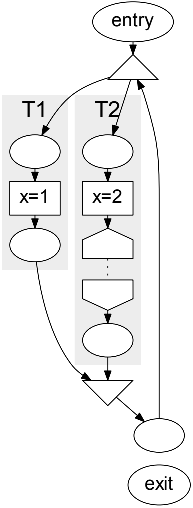
Thus, concurrency and (static) sequentiality are not **mutually exclusive, but orthogonal**!
However, (instantaneous) *run-time* sequentiality (on node *instances*) does exclude run-time concurrency



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- Like the synchronous MoC, the SC MoC ensures macro-tick determinacy by inducing certain scheduling constraints on variable accesses
- **Unlike** the synchronous MoC, the SC MoC tries to take **maximal advantage of the execution order already expressed by the programmer** through sequential commands
- A scheduler can only affect the order of variable accesses through **concurrent** threads

Notes on Free Scheduling II

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Similarly, threads are not concurrent with parent thread

- Because of path ordering $\prec$, a parent thread is always suspended when a child thread is in operation
- Thus, not up to scheduler to decide between parent and child thread
- No race conditions between variable accesses performed by parent and child threads; no source of non-determinacy

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In the following, will define such a restriction:
the SC-admissible schedules

Guideline for SC-admissibility

- Initialize-Update-Read protocol, for concurrent accesses
- Want to conservatively extend Esterel's "Write-Read protocol" (must do emit *before* testing)
- But does Esterel *always* follow write-read protocol?

Write After Read Revisited

```
module WriteAfterRead
output x, y, z;

emit x;
[
 present x then
   emit y
 end
||
 present y then
   emit z
 end;
 emit x
]
end
```

Esterel version

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Esterel version

```
module WriteAfterRead
output int x, y, z;
{
  x = 1;
  fork
    y = x;
  par
    z = y;
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SCL version

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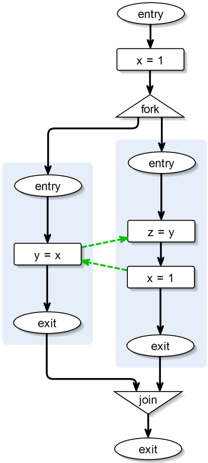

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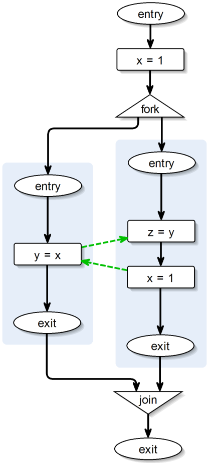

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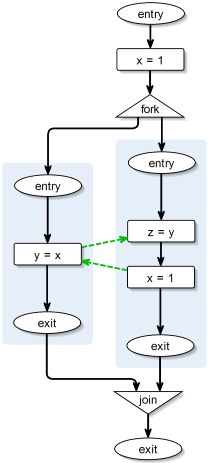

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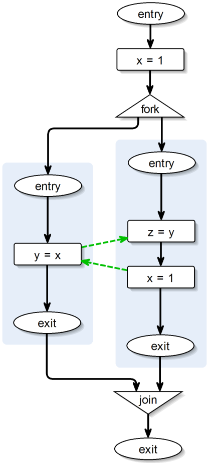

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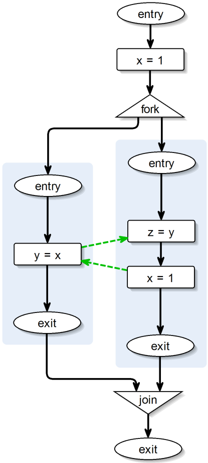

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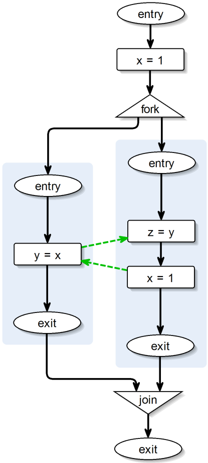

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```
module InEffective1
output int x = 2;
 int y;
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- → Strengthen notion of "ineffective writes":
- Consider writes "ineffective" only if they do not change read!

Ineffectiveness – 2nd Try

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```
module InEffective2
output bool x = false;
 int y;
{
 fork
   if (!x) {
     y = 1;
     x = x xor true
   }
   else
     y = 0
 par
   x = x xor true;
 join
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“x = x xor true”

- Relative writes
- Equivalent to “x = !x”

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- → Replace "ineffectiveness" by "confluence"

Overview

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- by symmetry $\rightarrow_{ww}$ implies $\leftrightarrow_{ww}$

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Given:

- Valid configuration (C, M) of SCG
- Nodes $n_1, n_2 \in N$

n_1, n_2 are conflicting in (C, M) iff

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Observations I

- Confluence is taken *relative* to valid configurations (C, M) and *indirectly* as the absence of conflicts
- Instead of requiring that confluent nodes commute with each other for *arbitrary* memories, we only consider those configurations (C', M') that are *reachable* from (C, M)
- *E. g.*, if it happens for a given program that in all memories M' reachable from a configuration (C, M) two expressions ex_1 and ex_2 evaluate to the same value, then the assignments $\mathrm{x} = ex_1$ and $\mathrm{x} = ex_2$ are confluent in (C, M)

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Observations II

- Similarly, if the two assignments are never jointly active in any reachable continuation pool C', they are confluent in (C, M), too
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- Thus, statements may be confluent for some program relative to some reachable configuration, but not for other configurations or in another program
- However, notice that relative writes of the same type are confluent in the absolute sense, *i. e.*, for all valid configurations (C, M) of all programs

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- Confluence $n_1 \sim_{(C,M)} n_2$ requires conflict-freeness for *all* configurations (C', M') reachable from (C, M) by *arbitrary* micro-sequences under *free scheduling*
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- Exploit this in following definition of confluence *of node instances* by making confluence of node instances within a macro tick relative to the index position at which they occur

Confluence of Node Instances [Def. 4.5]

Given:

- Macro tick R
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- for $i = min(i_1, i_2) - 1$
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- Q: Are L6 and L13 confluent?

InEffective2 Revisited

```
1  module InEffective2
2  output bool x = false;
3   int y;
4  {
5   fork
6     if (!x) {
7       y = 1;
8       x = x xor true
9     }
10    else
11      y = 0
12  par
13    x = x xor true;
14  join
15 }
```

Recall sequence L6; L7; L8; L13:

- Q: Is L13 ineffective *relative to L6*?
- A: Yes!
- L13 is out-of-order ...
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→ Def. of SC-admissibility – specifically, the underlying scheduling relations – uses confluence condition

Scheduling Relations [Def 4.6]

Given:

- Macro tick R with
- Node instances $ni_{1,2} = (n_{1,2}, i_{1,2})$, *i. e.*, $1 \leq i_{1,2} \leq len(R)$ and $n_{1,2} = R(i_{1,2})$
- $ni_{1,2}$ concurrent in R, *i. e.*, $ni_1 \mid_R ni_2$
- $ni_{1,2}$ not confluent in R, *i. e.*, $ni_1 \not\sim_R ni_2$

Then:

- $ni_1 \rightarrow^R_\alpha ni_2$ iff $n_1 \rightarrow_\alpha n_2$ for some $\alpha \in \alpha_{iur}$
- $ni_1 \rightarrow^R ni_2$ iff $i_1 < i_2$; *i. e.*, ni_1 happens before ni_2 in R.

Sequential Admissibility [Def. 4.7]

A macro tick R is SC-admissible iff

- for all node instances $ni_{1,2} = (n_{1,2}, i_{1,2})$ in R, with $1 \leq i_{1,2} \leq len(R)$ and $n_{1,2} = R(i_{1,2})$,
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the scheduling condition SC_α holds:
if $ni_1 \rightarrow^R_\alpha ni_2$ then $ni_1 \rightarrow^R ni_2$.

A run for an SCG is SC-admissible if all macro ticks R in this run are SC-admissible.

SC-admissibility vs. Determinacy

SC-admissibility vs. Determinacy

```
module NonDet
output bool x = false, y = false;
{
 fork { // Thread CheckX
  if (!x)
   y = true;
 }
 par { // Thread CheckY
  if (!y)
   x = true
 }
 join
}
```

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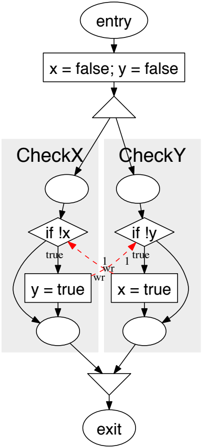

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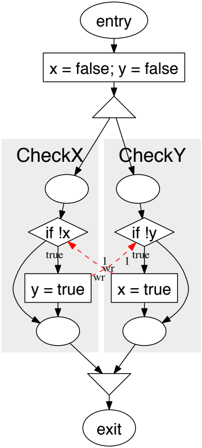

- Admissible runs? Yes, multiple
- Determinate? No

Thus: **SC-admissibility $\not\Rightarrow$ Determinacy**

SC-admissibility vs. Determinacy

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module Fail
output bool z = false;
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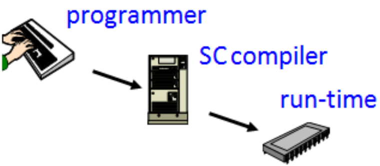
- Determinate? Yes

Thus: **Determinacy $\not\Rightarrow$ SC-admissibility**

Sequential Constructiveness [Def. 4.8]



Definition: A program P is sequentially constructive (SC) iff for each initial configuration and input sequence:

1. There exists an SC-admissible run (P is reactive)
2. Every SC-admissible run generates the same determinate sequence of macro responses (P is determinate)

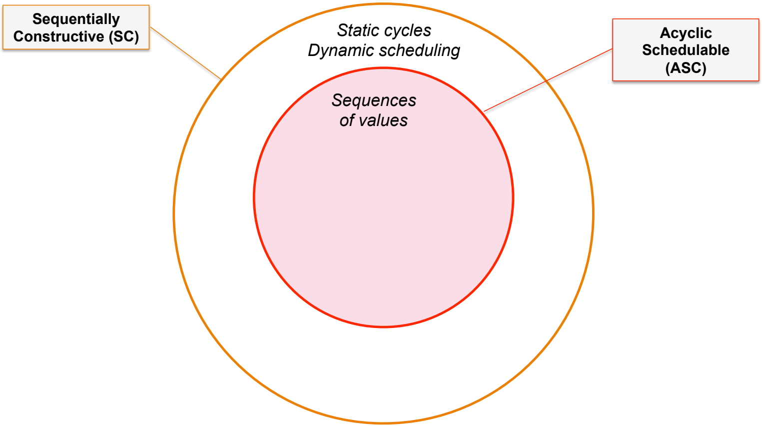
Overview

Motivation

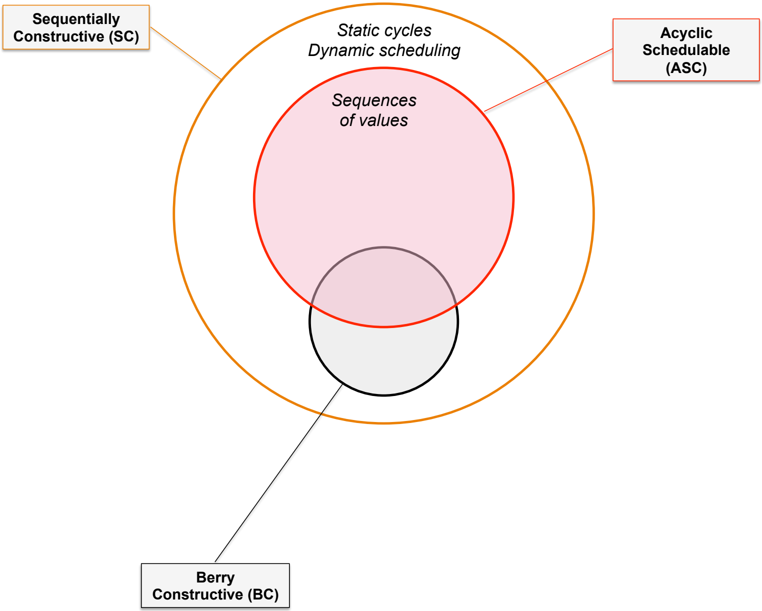
Formalizing Sequential Constructiveness (SC)

Wrap-Up
- Synchronous Program Classes
- Summary

Synchronous Program Classes [TR, Sec. 9]



Synchronous Program Classes [TR, Sec. 9]



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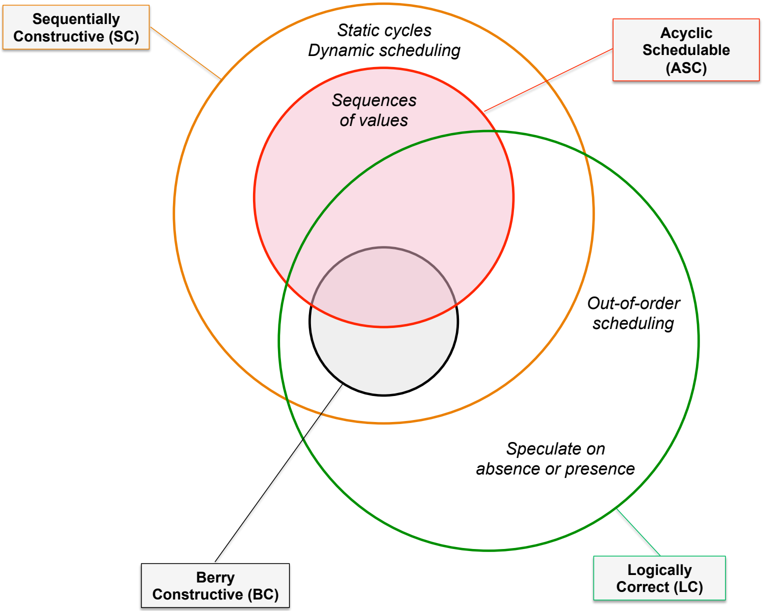

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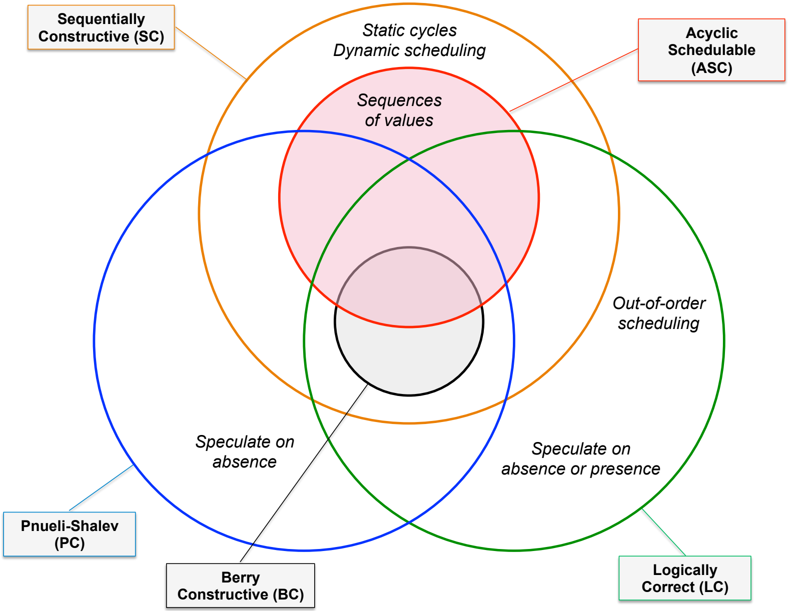

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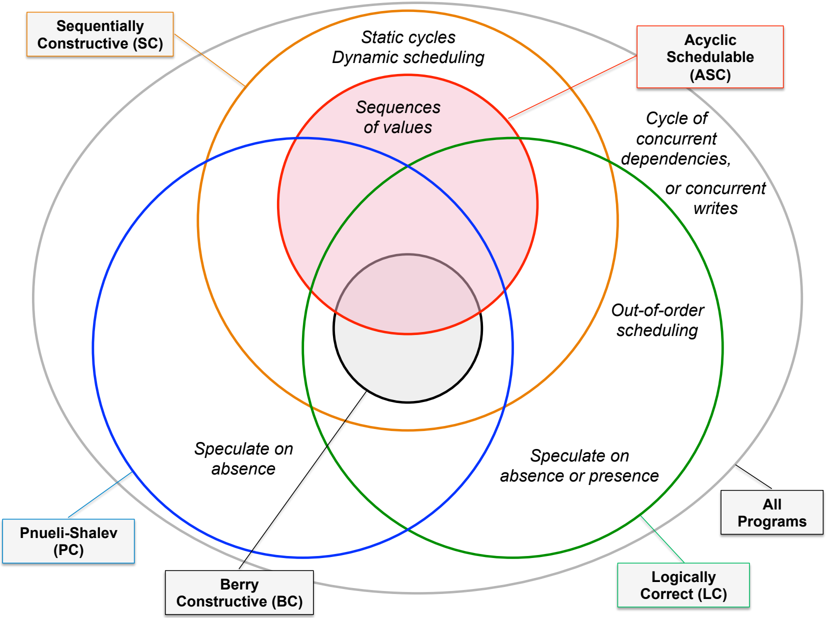

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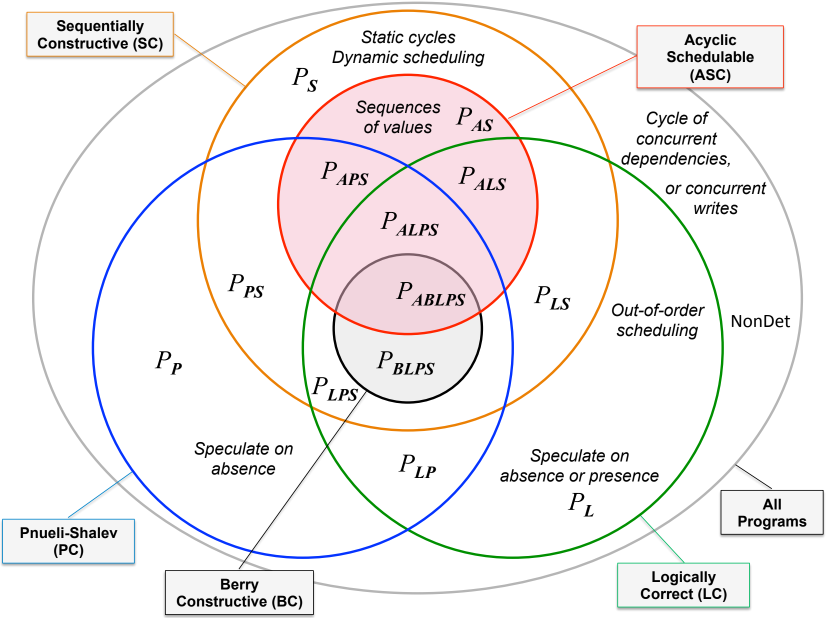

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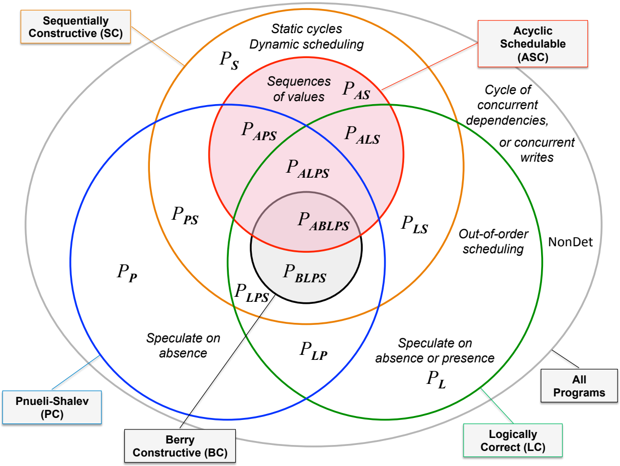
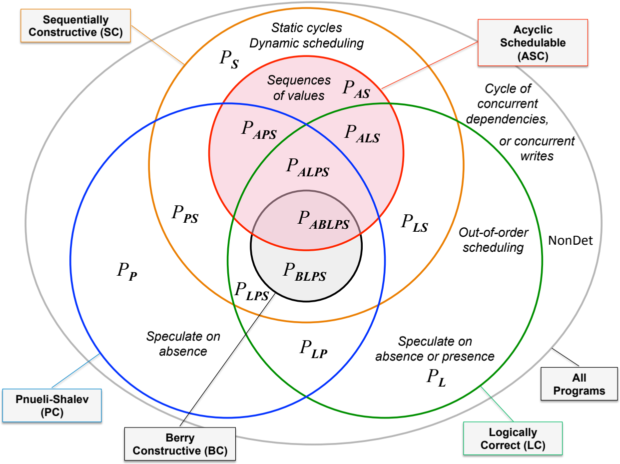


Example $P_{APS} =$

Synchronous Program Classes



Example P_{APS} = if (x) x = 1

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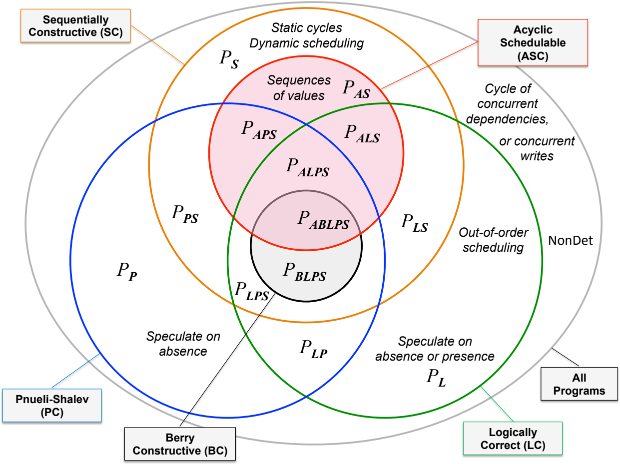

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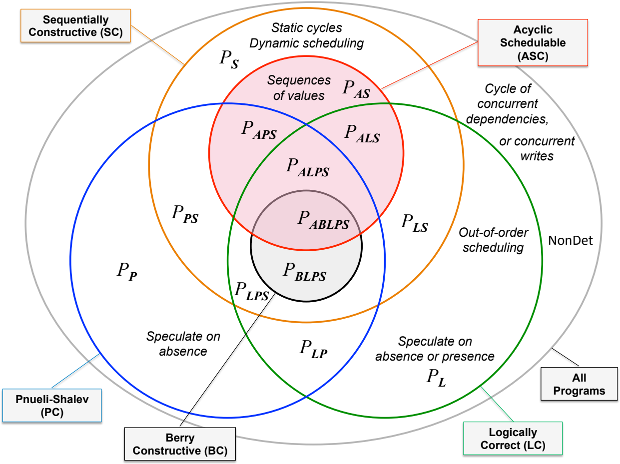
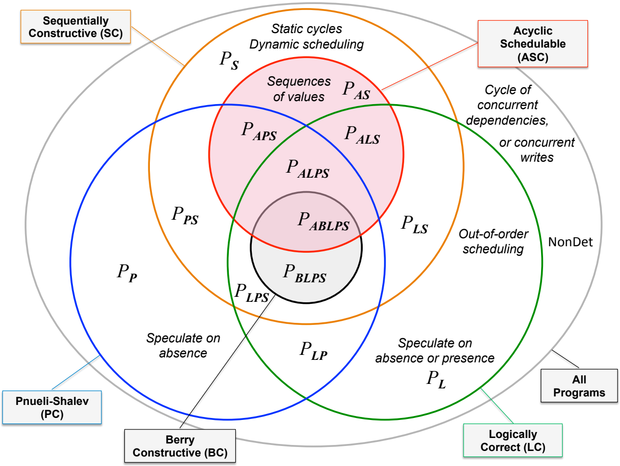


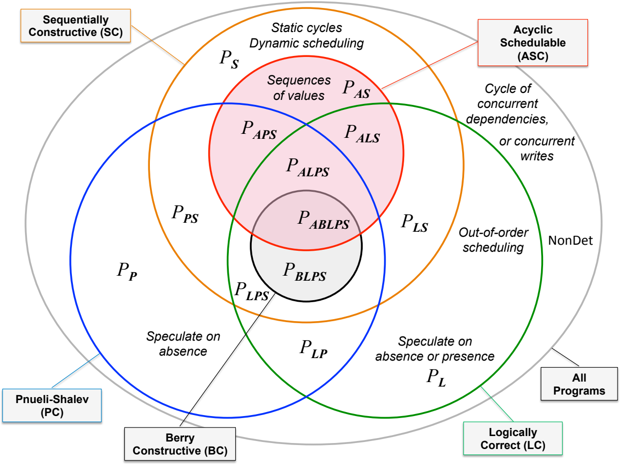
Example P_{AS} = if (!x) x = 1

Synchronous Program Classes



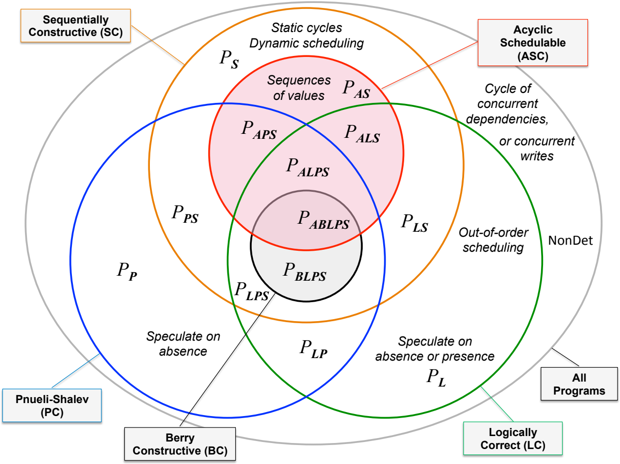
Example $P_{ALS} =$

Synchronous Program Classes



Example P_{ALS} = if (!x) x = 1 else x = 1

Synchronous Program Classes



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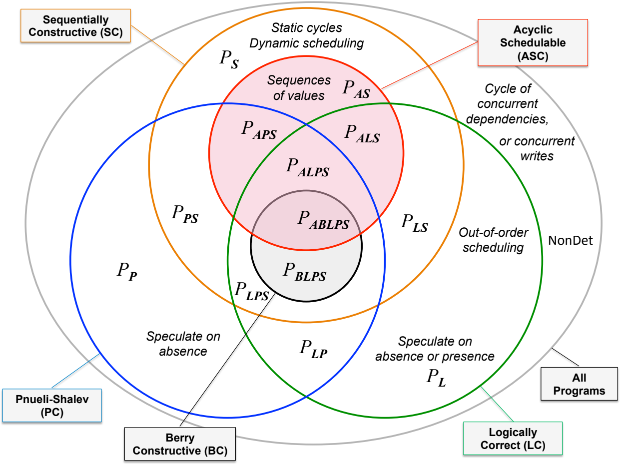

Example P_{ALPS} = if (!x && y) {x = 1; y = 1}

Summary

Underlying idea of sequential constructiveness rather simple

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- Prescriptive instead of descriptive sequentiality
- Thus circumventing "spurious" causality problems
- Initialize-update-read protocol

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However, precise definition of SC MoC not trivial

- Challenging to ensure conservativeness relative to Berry-constructiveness
- Plain initialize-update-read protocol does not accomodate, *e. g.*, signal re-emissions
- Restricting attention to *concurrent*, *non-confluent* node instances is key

Conclusions

- Clocked, **synchronous model of execution** for **imperative, shared-memory multi-threading**
- Conservatively extends synchronous programming (Esterel) by **standard sequential control flow** (Java, C)
- $\Longrightarrow$ Deterministic concurrency with synchronous foundations, but without synchronous restrictions
  - ☺ Expressive and intuitive sequential paradigm
  - ☺ Predictable concurrent threads

Future Work

Plenty of extensions/adaptations possible ...

- Alternative notions of sequential constructiveness:
  - A truly "constructive" approach that sharpens SC admissibility to determinate schedules
  - Extension of iur-protocol, *e. g.*, to model ForeC
- Improved synthesis & analysis — see also next lecture