Synchronous Languages—Lecture 07

Prof. Dr. Reinhard von Hanxleden

Christian-Albrechts Universität Kiel
Department of Computer Science
Real-Time Systems and Embedded Systems Group

20 Nov. 2018

Last compiled: November 18, 2018, 16:52 hrs

Esterel V—The Constructive Circuit Semantics
The 5-Minute Review Session

1. What is the derivative (Ableitung) of a program?
2. How is the program transition of an Esterel program defined?
3. How do program transitions express logical coherence?
4. Which semantics for Esterel exist?
5. What are the constructive coherence laws, how do they differ from the logical coherence law?
Overview

The Circuit Semantics
Constructive circuits
The basic circuit translation
Translating the Esterel kernel
The Circuit Semantics

Translating Esterel to Circuits

- Can consider Esterel programs as SW or HW descriptions
- As it turns out, the HW-equivalent of constructiveness is that the synthesized circuit is delay-independent
  - This gives a firm, physical base for the constructive semantics we just considered
- Can in turn simulate this synthesized HW-circuit in SW
  - This is just what the Esterel v5 compiler does
  - Can then also take advantage of HW optimization techniques
  - Use BDD-based techniques to check constructiveness
Circuit Semantics—Introduction

-module P1:
  input I;
  output O;
  signal S1, S2 in
    present I then emit S1 end ||
    present S1 else emit S2 end ||
    present S2 then emit 0 end
  end signal
end module

circuit C1:
  S1 = I
  S2 = ¬S1
  O = S2

- Resulting circuit is acyclic
- Hence always stabilizes
- Reactive and deterministic
Circuit Semantics—Introduction

module P3:
output O;
present 0 else emit 0 end
end module

≡
circuit C3:
O = ¬O

▶ Resulting circuit never stabilizes
▶ Not reactive
Circuit Semantics—Introduction

module P4:
output 0;
present 0 then emit 0 end
end module

≡
circuit C4:
O = O

- Resulting circuit can stabilize at different values
- Not deterministic
Circuit Semantics—Introduction

module P9:
[
    present 01 then emit 01 end
||
    present 01 then
    present 02 else emit 02 end
end

≡

circuit C9:
O1 = 01
O2 = O1 \land \neg O2

▶ Reactive and deterministic
▶ But not constructive!
Circuit Semantics—Introduction

module P12:
    present 0 then
        emit 0;
    else
        emit 0
    end

≡

\[
O = O \lor \neg O
\]

≡

Reactive and deterministic

Meaning: If it stabilizes, there is only one possible value for each wire’s voltage

But: Does it always stabilize?
Circuit Semantics—Introduction

- Consider following delay assignment:

- Circuit is reactive and deterministic (Newtonian model)
- But: Circuit never stabilizes (Vibration model)
- Hence: Electrical stabilization is not the conjunction of reactivity and determinism!
Circuit Semantics—Introduction

module P13:
present I then
  present 02 then emit 01 end
else
  present 01 then emit 02 end
end

circuit C13:
O1 = I \land O2
O2 = \neg I \land O1

- Reactive and deterministic
- Cyclic, yet always stabilizes
- **Hence:** Electrical stabilization does not require acyclicity
- **In fact:** Electrical stabilization equivalent to constructiveness
Constructive Circuits

Basic building blocks

- Allow insertion of arbitrary delays
- Registers:
  - \( \text{reg}(X) = 0 \rightarrow \text{pre}(X) \)
Constructive Circuits

Constructive Boolean (intuitionistic) logic:

- Evaluate equations with constant folding rules
  - not 0 → 1
  - not 1 → 0
  - 1 or x → 1
  - x or 1 → 1
  - 0 or 0 → 0
  - 0 and x → 0
  - x and 0 → 0
  - 1 and 1 → 1

- There is no law of excluded middle (x or not x → 1)!
- Circuit equations yield solution iff circuit is delay insensitive (i.e., the original Esterel program is constructive)
  - Propagation of 1’s corresponds to *Must*-analysis
  - Propagation of 0s corresponds to *Cannot*-analysis
The Basic Circuit Translation

- Structural translation
- Follows state semantics
  - Associate registers with “1” statements (pause)
  - Associate combinational logic with all other statements
  - Build up program-circuit from subcircuits
  - Additional boot register to implement initial state
- Basic circuit translation does not address schizophrenia (see later)
Interface for subcircuits

Inputs:

▶ **GO**: Starts statement afresh
▶ **RES**: Resumes execution of a selected statement
▶ **SUSP**: Suspend execution of the statement
  ▶ Registers keep their current value unless killed because of the KILL input
▶ **KILL**: Unsets statement’s registers in case of a trap exit
Interface for subcircuits contd.

Outputs:

- **SEL**: Indicates that a state in statement is currently selected for resumption, i.e. that some internal pause register is set
  - Is simply the disjunction of the internal registers.
- **K0, K1, ...**: Completion codes (1-hot encoding)
Interface for subcircuits contd.

- **E** and **E'**: input/output signal interface
- Are compound pins or buses
  - Contain one elementary pin per signal visible in the scope of the current statement.
- May freely extract specific signals s or s' out of E or E'.
- As for the K pins, the E' pins are explicitly unset when the statement is not executed
  - i.e. when \( \neg ( \text{GO} \lor (\text{RES} \land \text{SEL})) \)
The Global Environment

- Boot register sets GO input in initial instant
- At each clock cycle
  - set RES
  - clock the registers
Translating the Esterel Kernel

- Completion, with $k \neq 1$:
  
  ![Circuit diagram for completion]

  \[\text{GO} \rightarrow \text{K0} \quad \text{code 0}\]
  \[\text{GO} \rightarrow \text{K2} \quad \text{code 2}\]

- $k = 1$ (pause):
  
  ![Circuit diagram for pause]

  \[\text{GO} \quad \text{K1}\]
  \[\text{RES} \quad \text{K0}\]
  \[\text{SUSP} \quad \text{SEL}\]
  \[\text{KILL}\]
Translating the Esterel Kernel

\[ \text{GO} \quad !s : \quad s' \quad \text{K0} \]
Translating the Esterel Kernel

\[ p ; q \]
Translating the Esterel Kernel

\[ s? p, q: \]
Translating the Esterel Kernel

\[ s \supset p: \]
Translating the Esterel Kernel

$p^*$:
Translating the Esterel Kernel

\[ p \parallel q: \]
The Circuit Semantics

Translating the Esterel Kernel

- $p \parallel q$ (contd):
  - The synchronizer computes the maximum of the completion codes
  - Implemented with this (constructive) circuit:
Translating the Esterel Kernel

\[ \{p\} : \]

---

The Circuit Semantics
Translating the Esterel Kernel

\[ p: \]
Translating the Esterel Kernel

▶ \( p/s: \)

![Diagram of circuit semantics for Esterel kernel translation]
Example

module P2:
signal S in
  emit S;
  present 0 then
    present S then
      pause
    end present;
  emit 0
end present
end signal

circuit C2:
B = ¬ REG(1)  // Boot
S = B
R = REG(B ∧ O ∧ S)  // pause
O = (B ∧ O ∧ ¬S) ∨ R
K0 = (B ∧ ¬O) ∨ (B ∧ O ∧ ¬S) ∨ R
K1 = B ∧ O ∧ S
To Go Further