Synchronous Languages—Lecture 13

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Sequentially Constructive Concurrency

The 5-Minute Review Session

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4. What are *basic blocks*? What are *scheduling blocks*?
5. When compiling from the SCG, what types of *low-level synthesis* do we distinguish? How do they compare?

Safety-Critical Embedded Systems

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- Computations often exploit *concurrency*
- Key challenge:
  Concurrency must be deterministic!

Thanks to Michael Mendler (U Bamberg) for support with these slides

Implementing (Deterministic) Concurrency

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Aim: Deterministic concurrency with synchronous foundations, but without synchronous restrictions.

Comparing Both Worlds

Sequential Languages

- C, Java, ...

Synchronous Languages

- Esterel, Lustre, Signal, SCADE, SyncCharts ...

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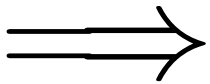

Sequentially Constructive Model of Computation (SC MoC)

- ☺ Deterministic concurrency and deadlock freedom
- ☺ Intuitive programming paradigm

Implementing Deterministic Concurrency: SC MoC

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- **Sequential** micro-step control flow

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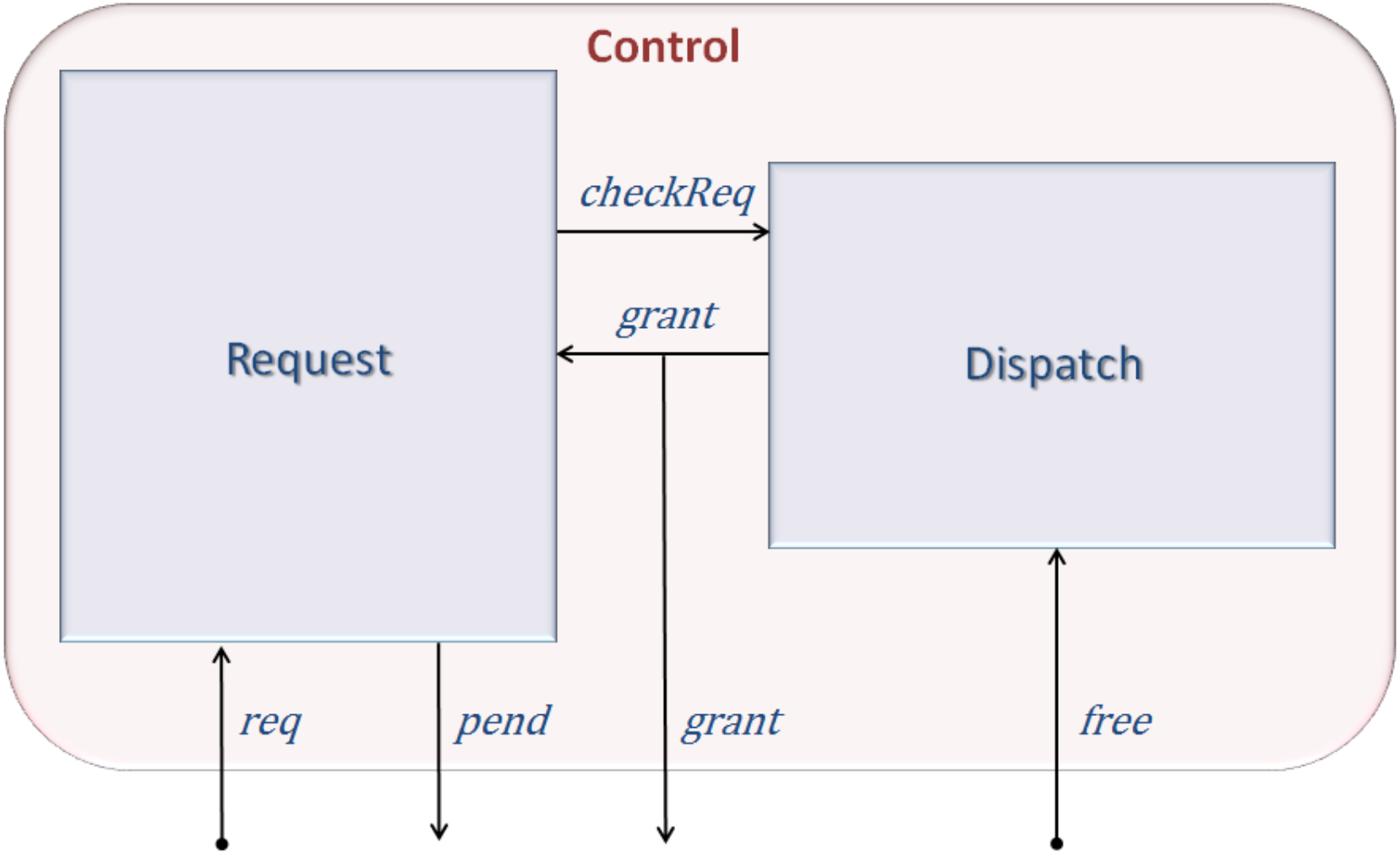
A Sequentially Constructive Program



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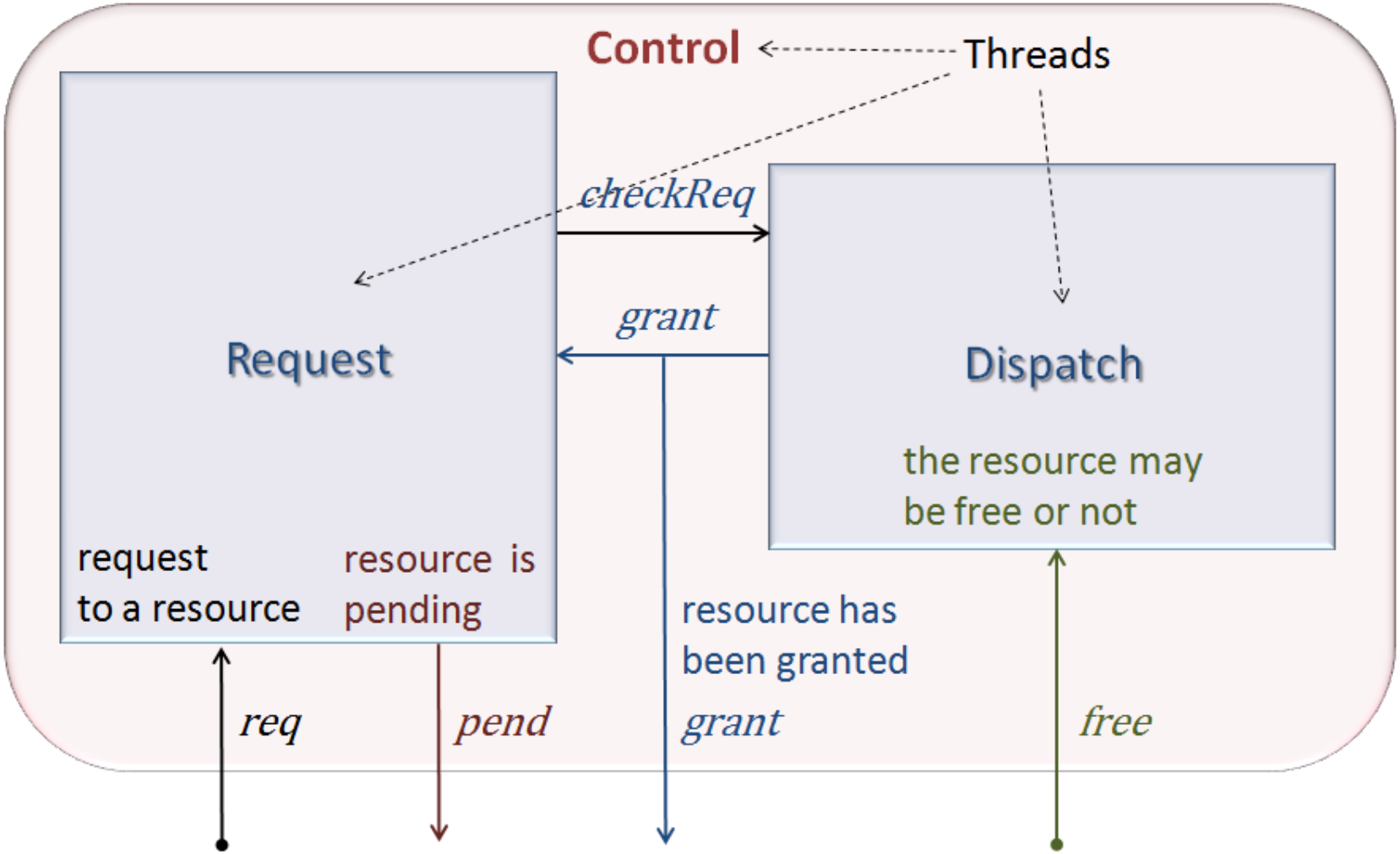

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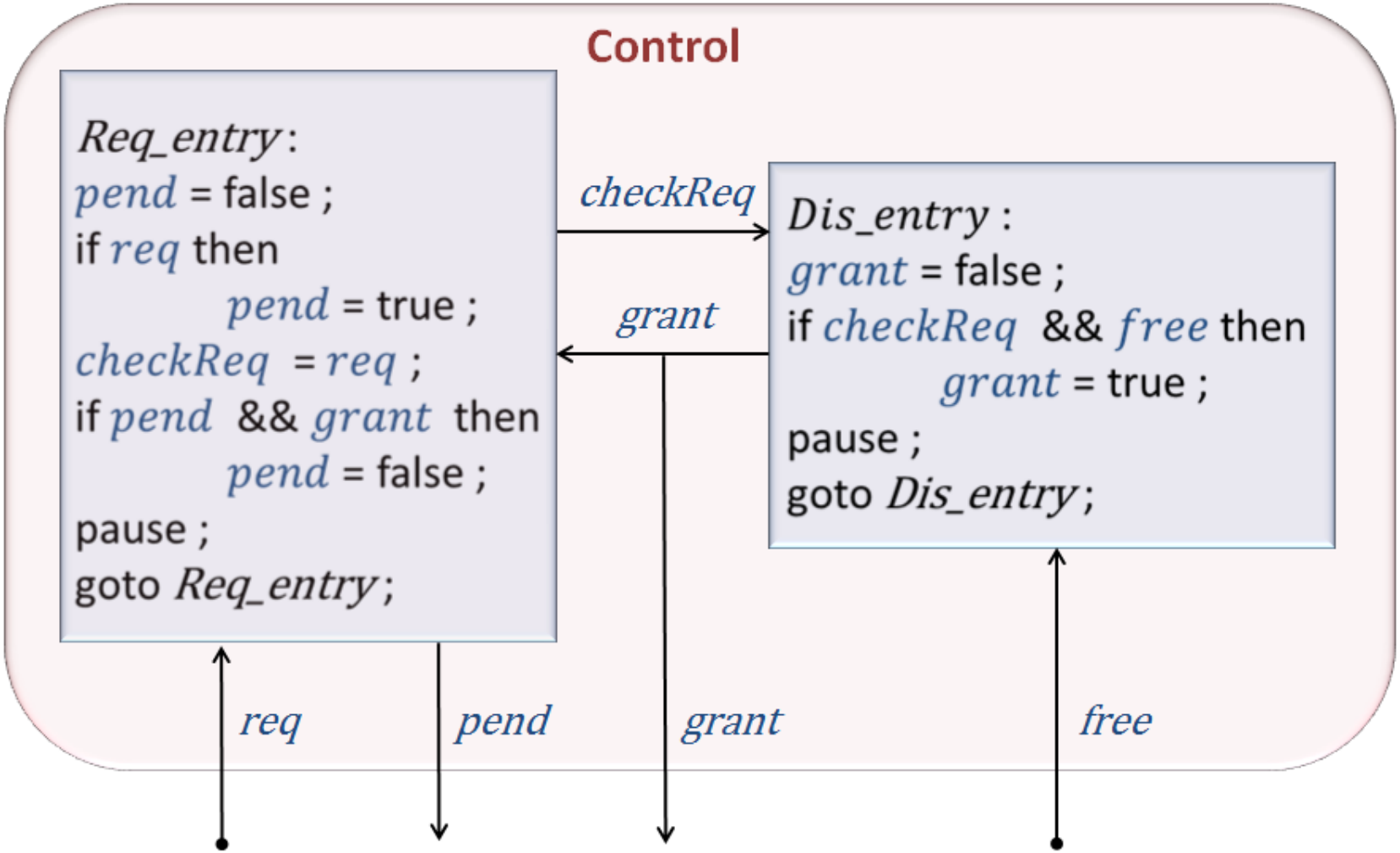

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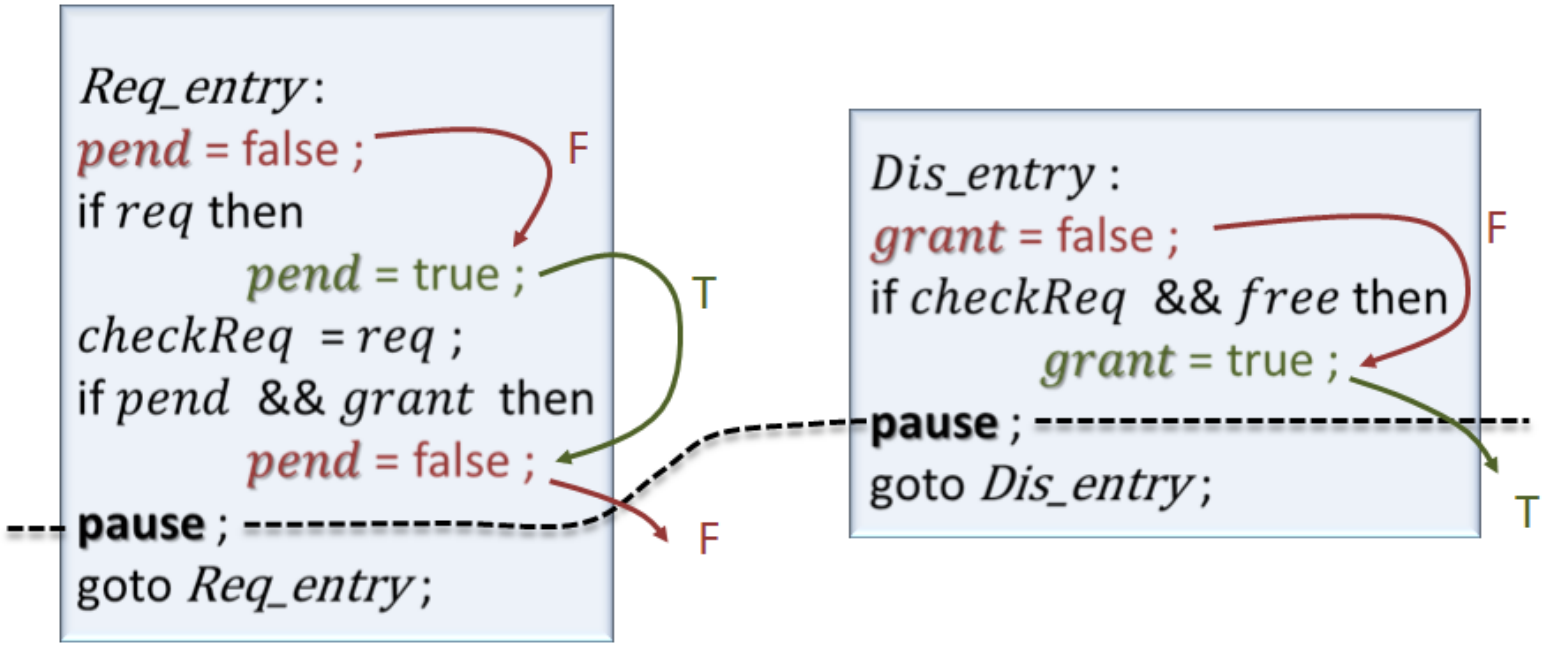

Imperative program order (sequential access to shared variables)

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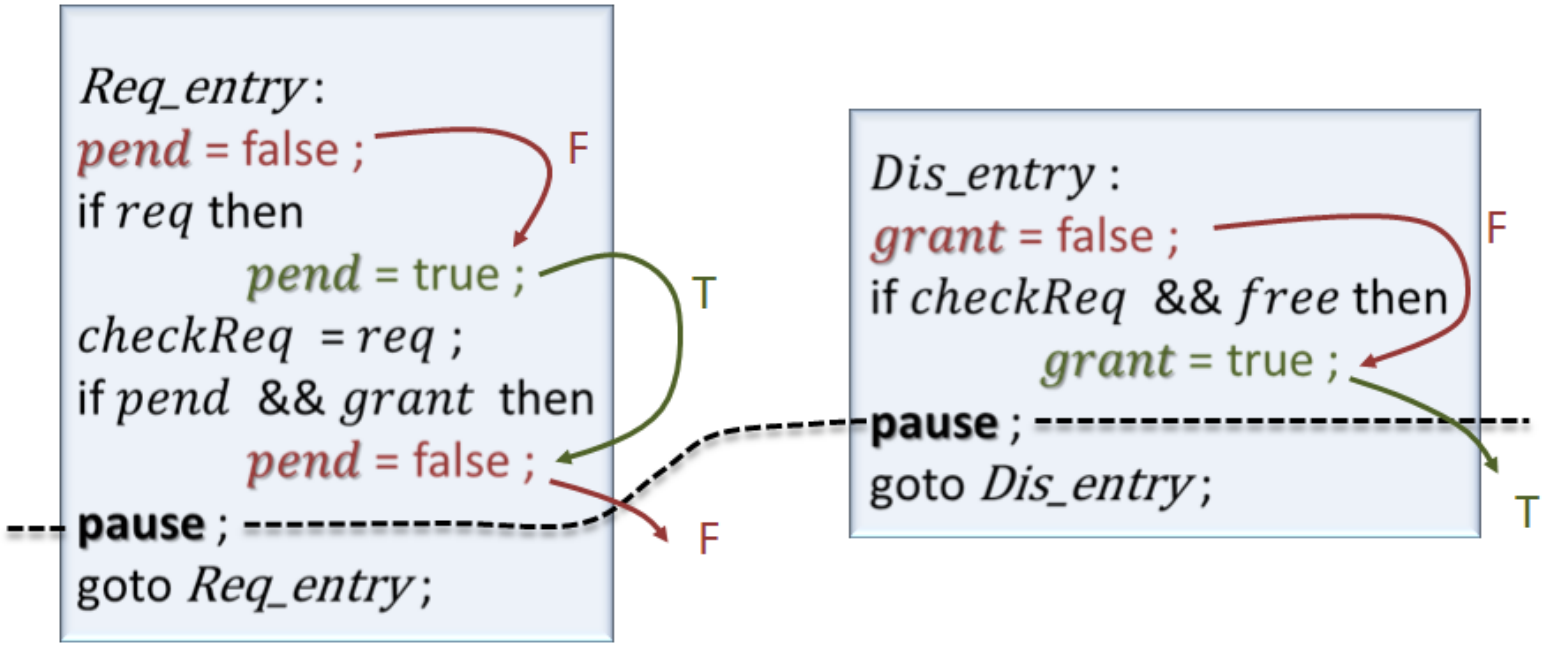

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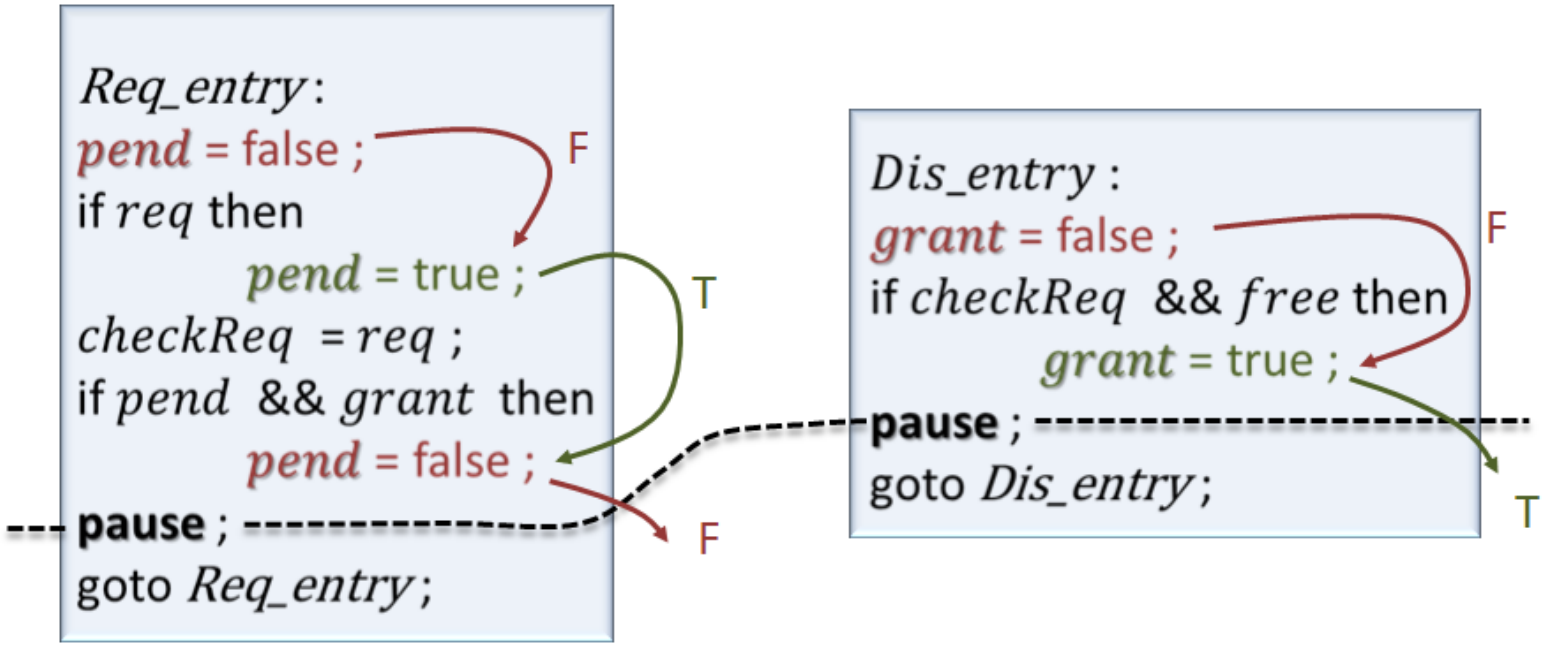

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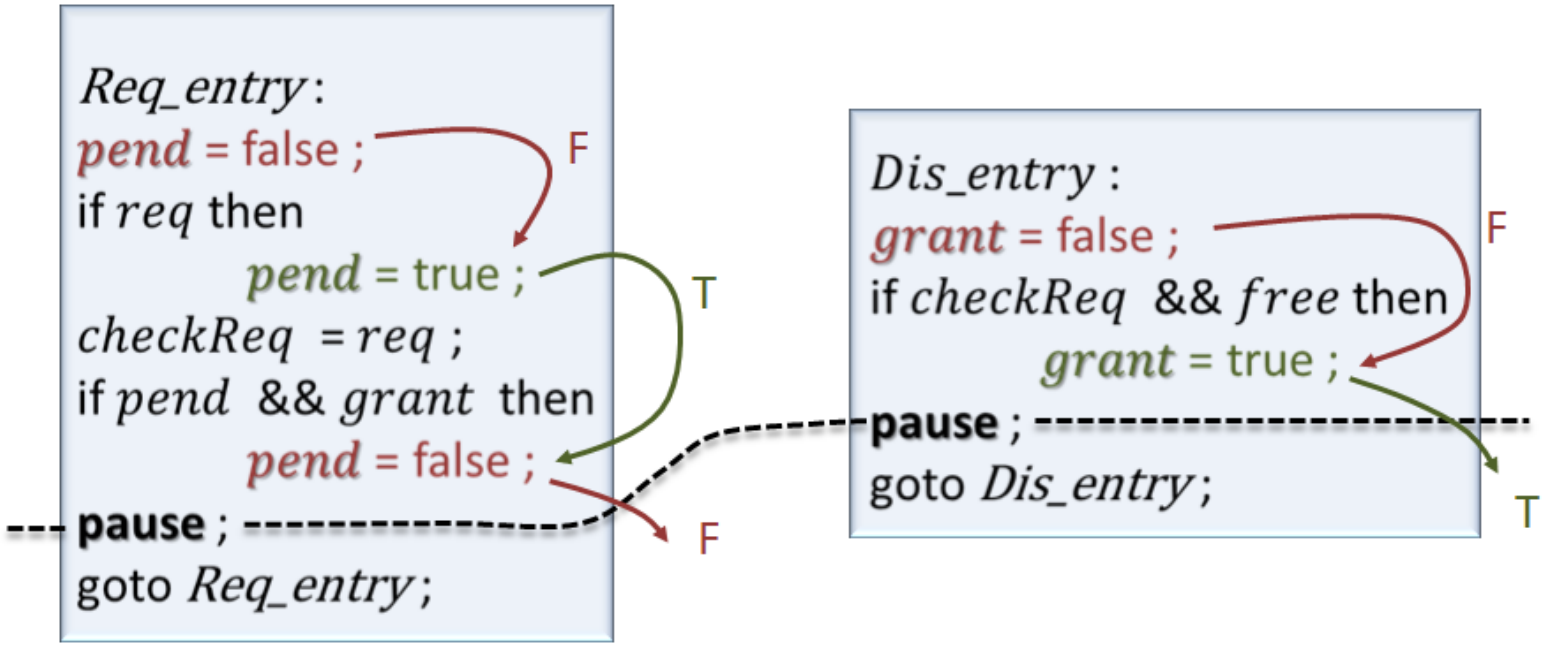

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  - ☺ Accepted in SC MoC
  - ☹ Not permitted in standard synchronous MoC

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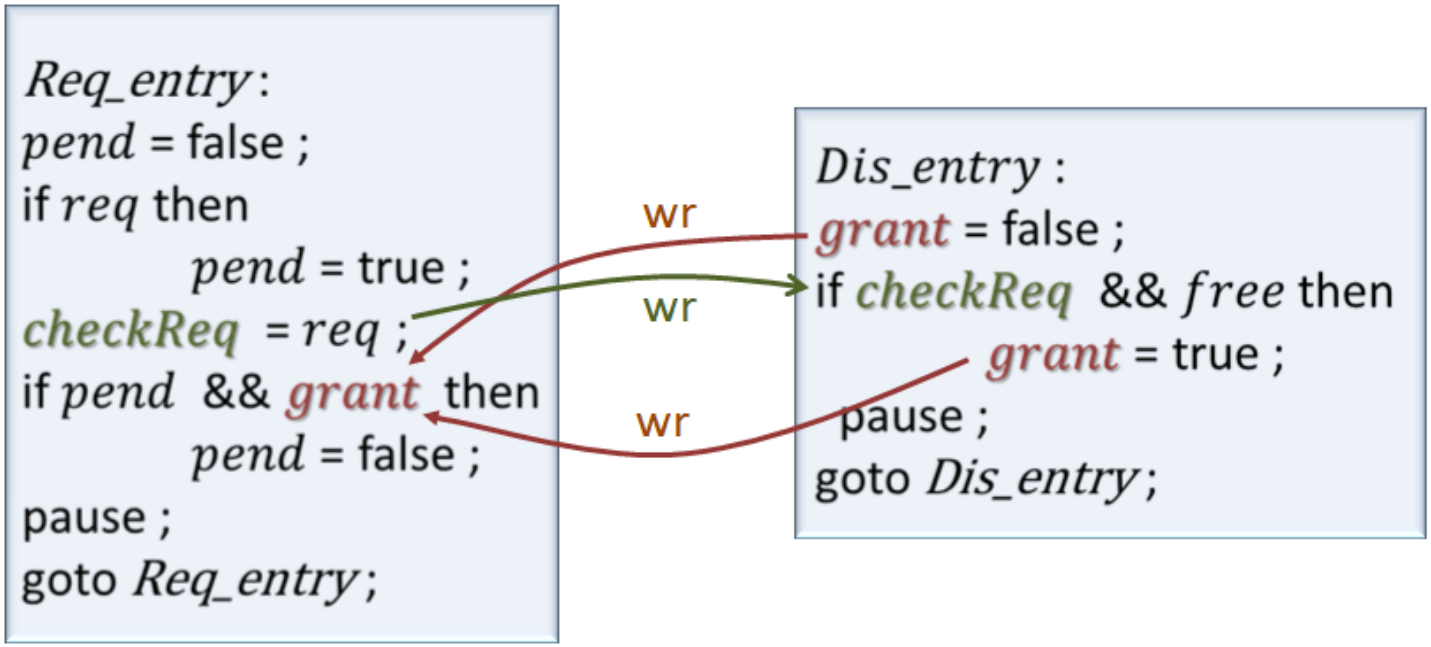

Concurrency scheduling constraints (access to shared variables):

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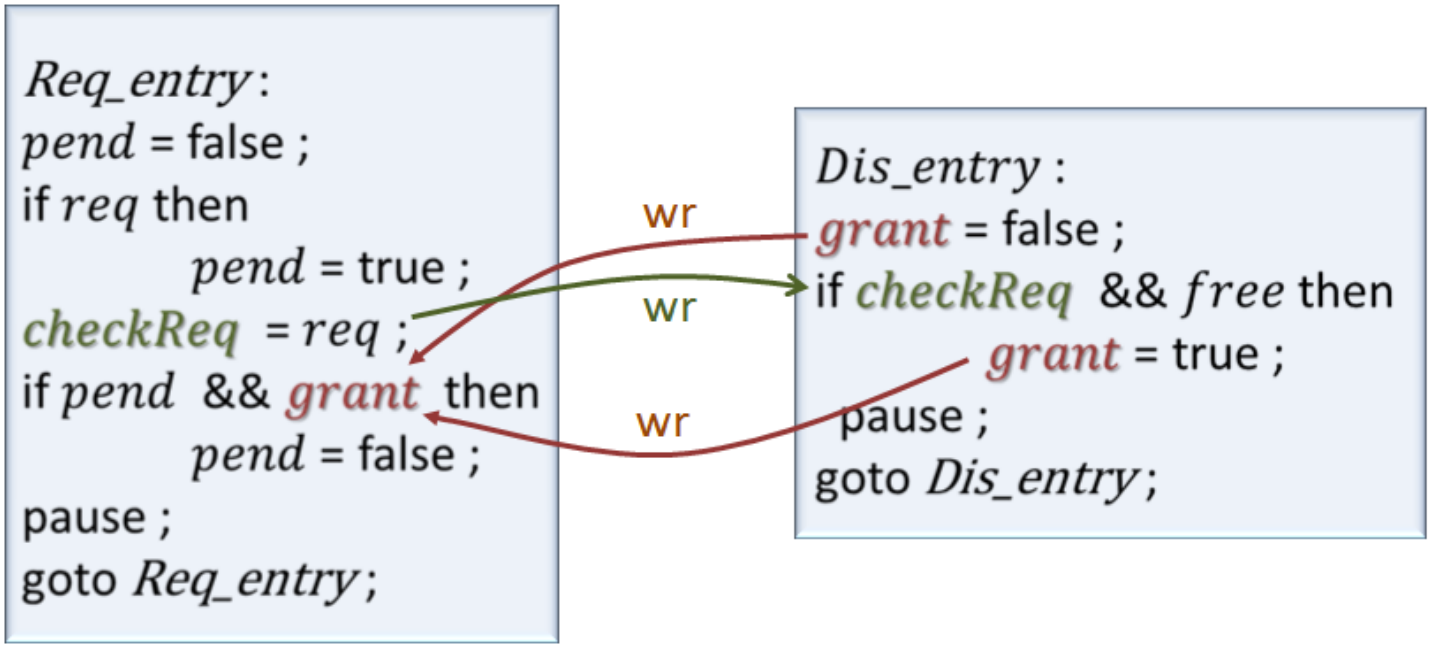

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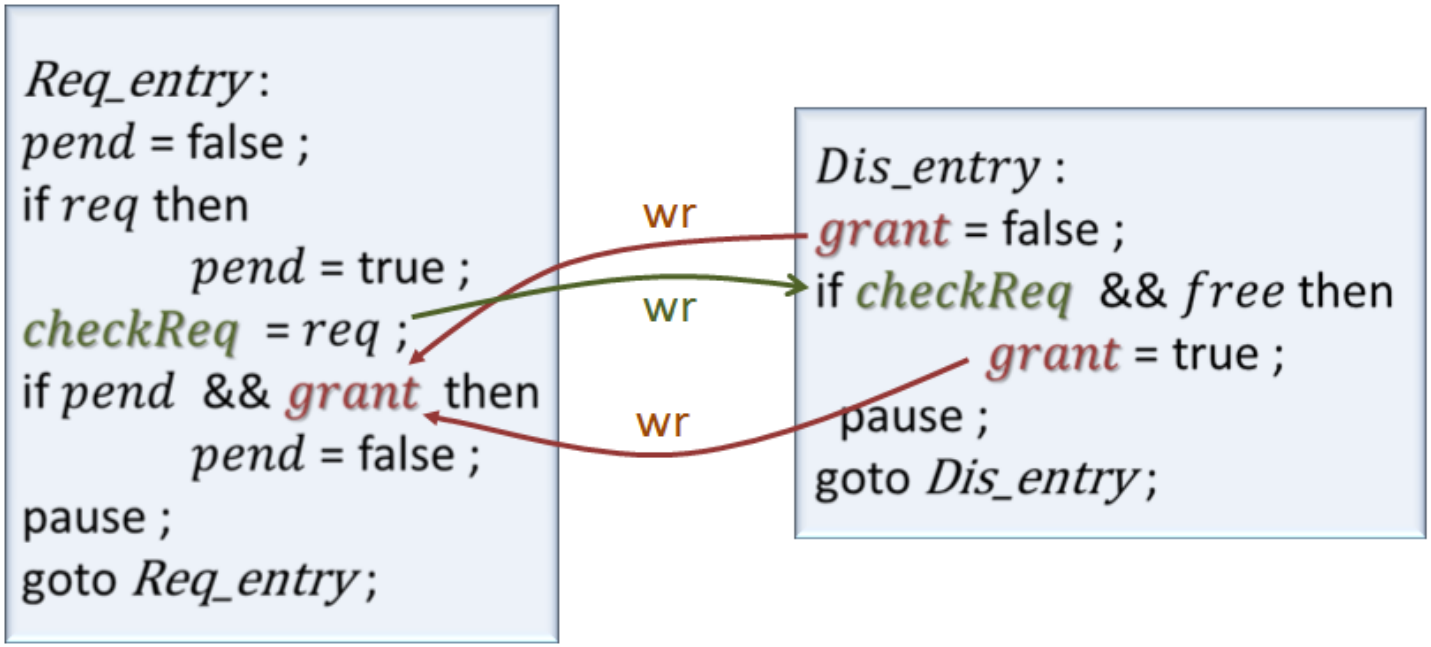

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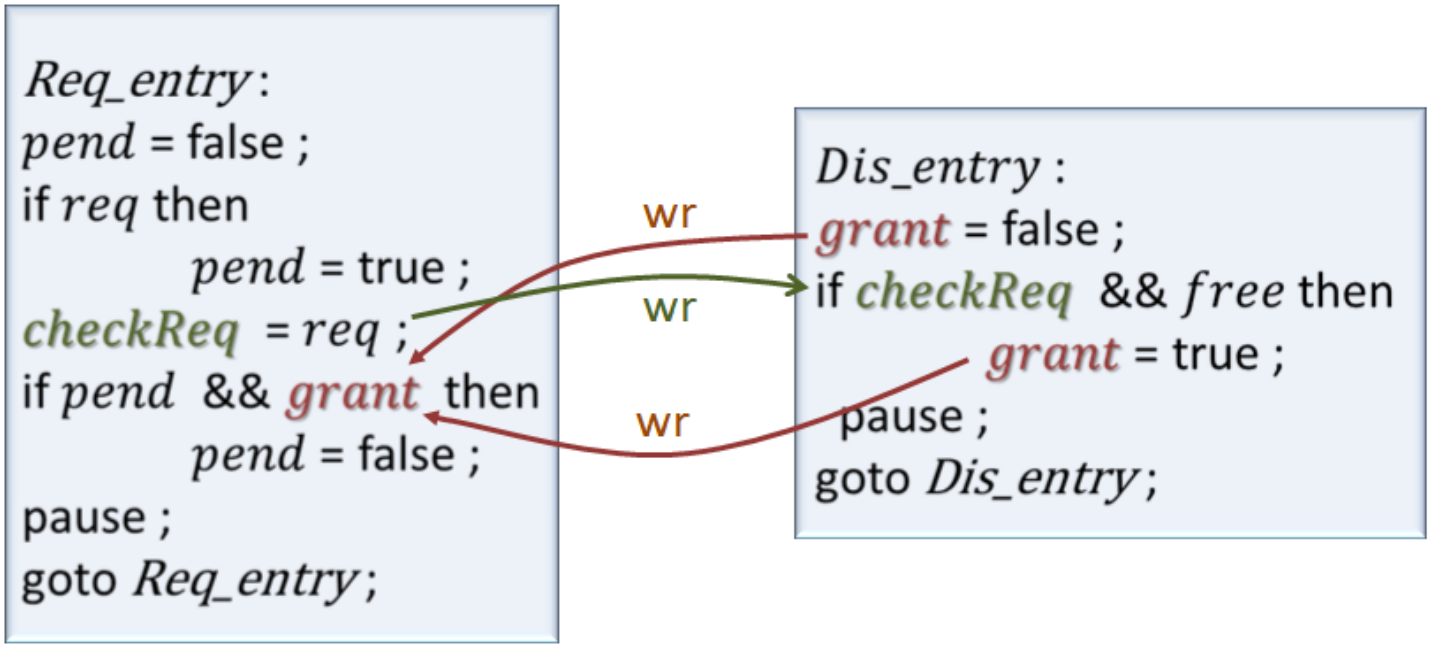

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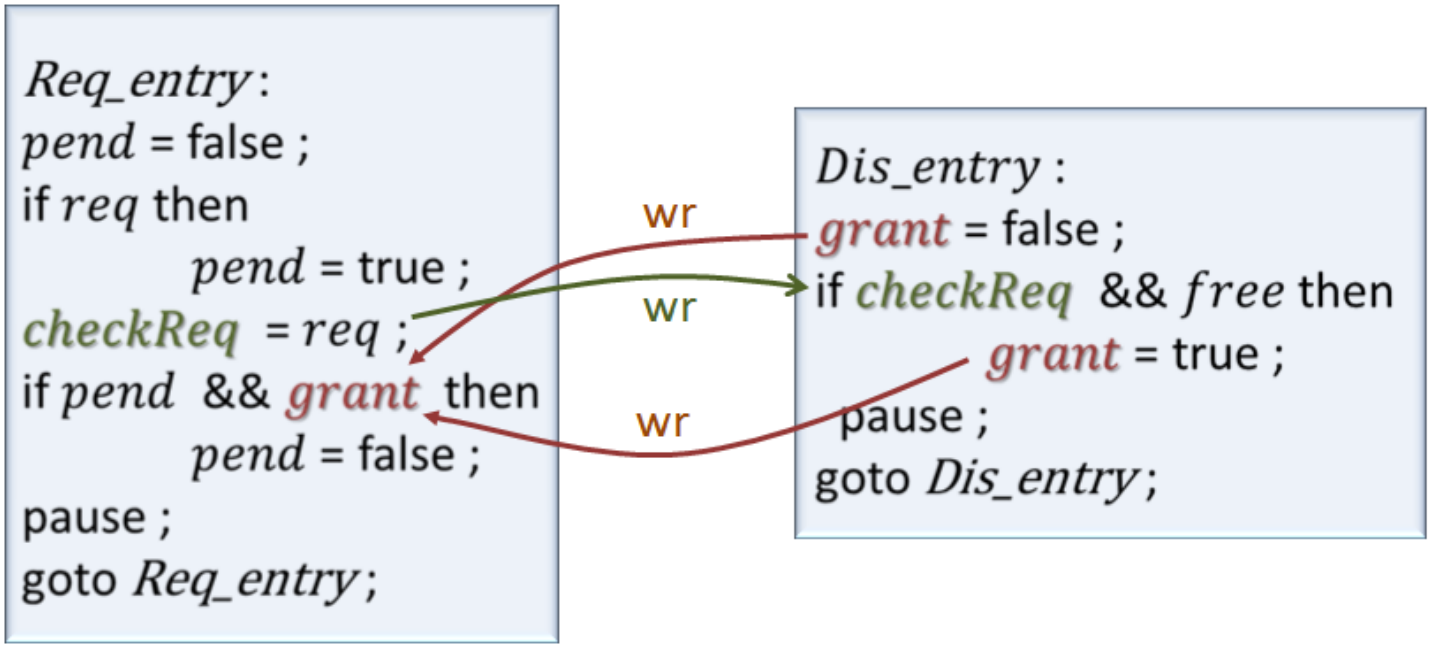

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- Implemented by the SC compiler

A Constructive Game of Schedulability

logically reactive program

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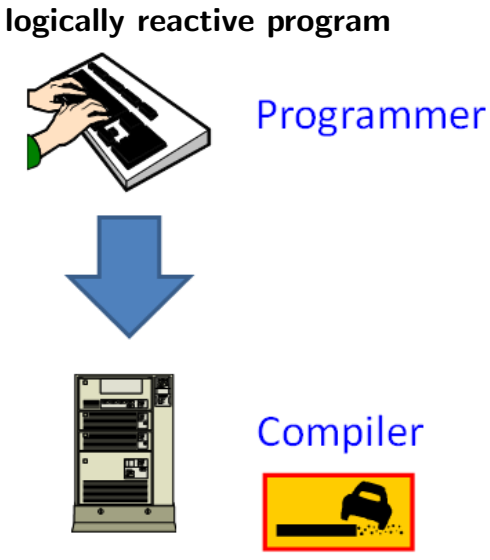

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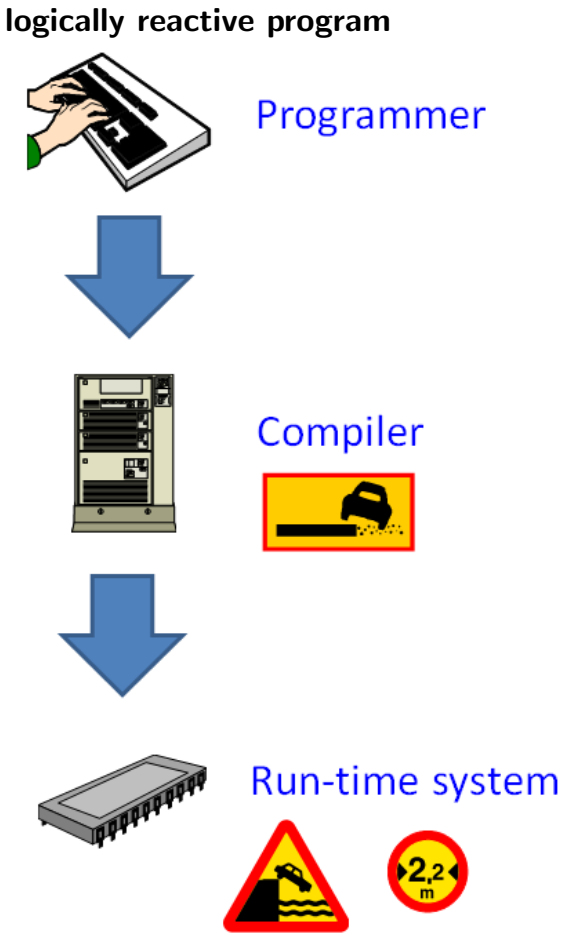

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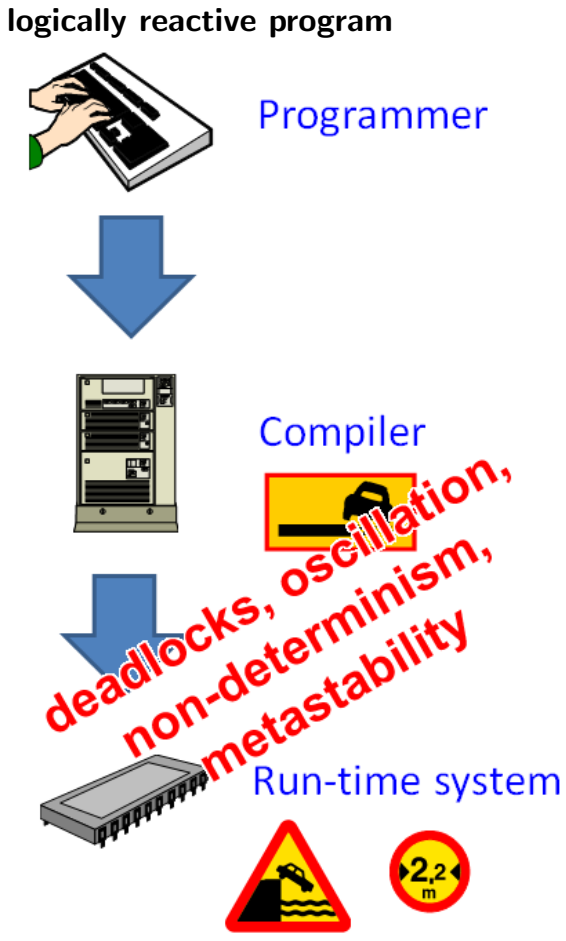

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The following applies to **concurrent** variable accesses only ...

Organizing Concurrent Variable Accesses

SC Concurrent Memory Access Protocol (per macro tick)

concurrent, multi-writer, multi-reader variables

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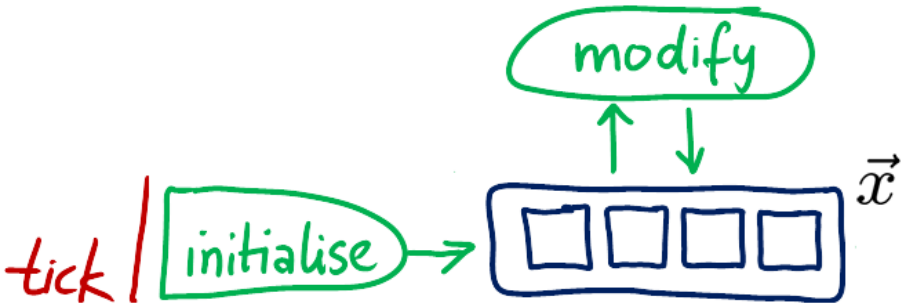

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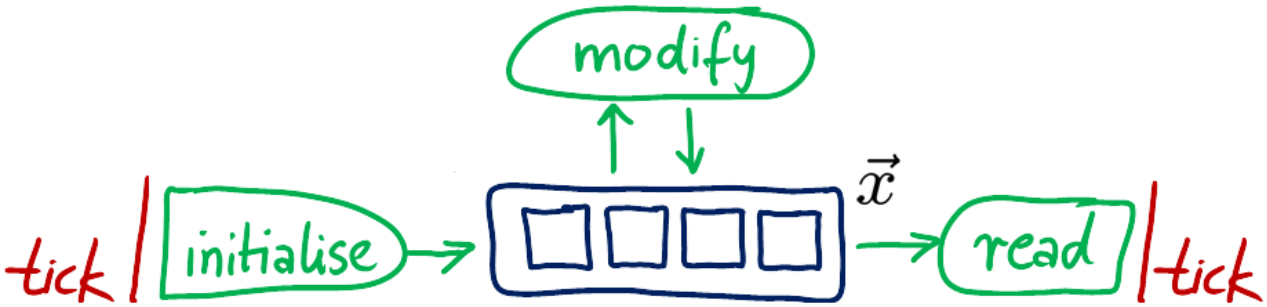

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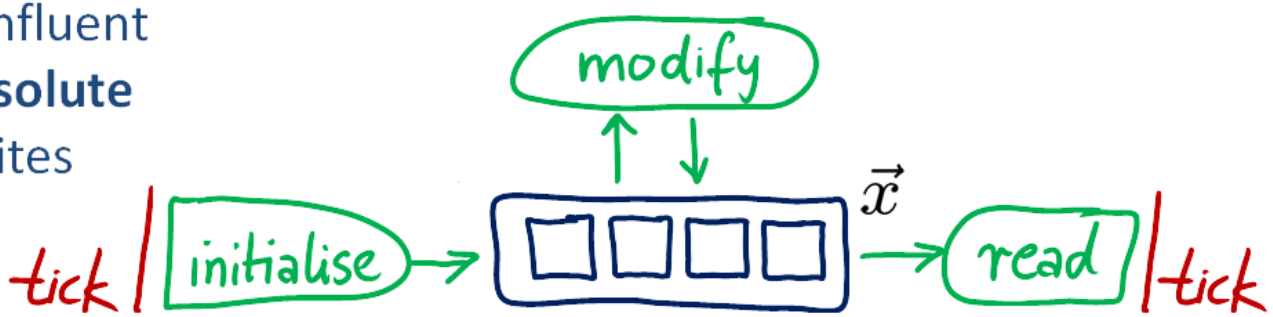
confluent
absolute
writes



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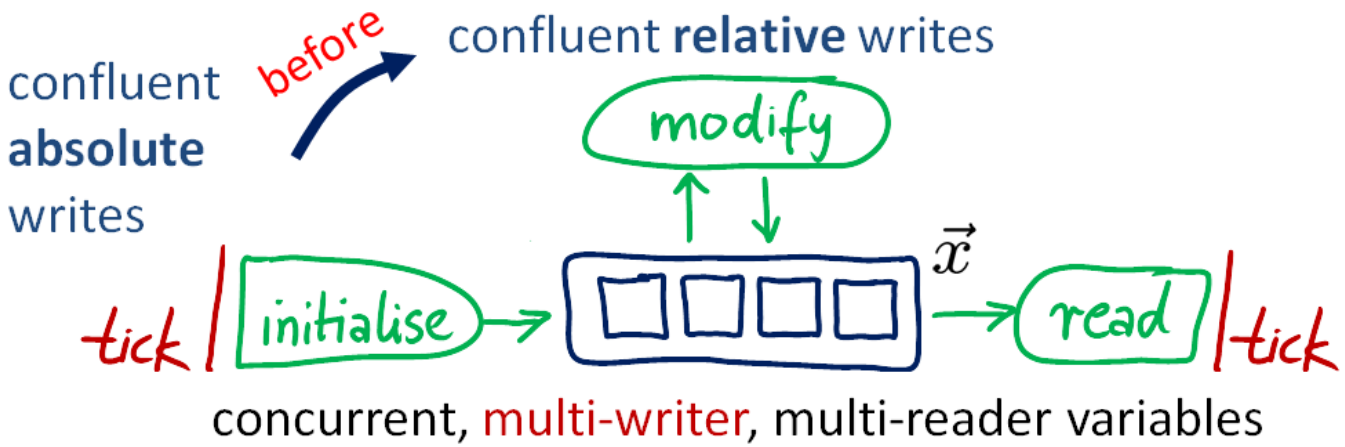

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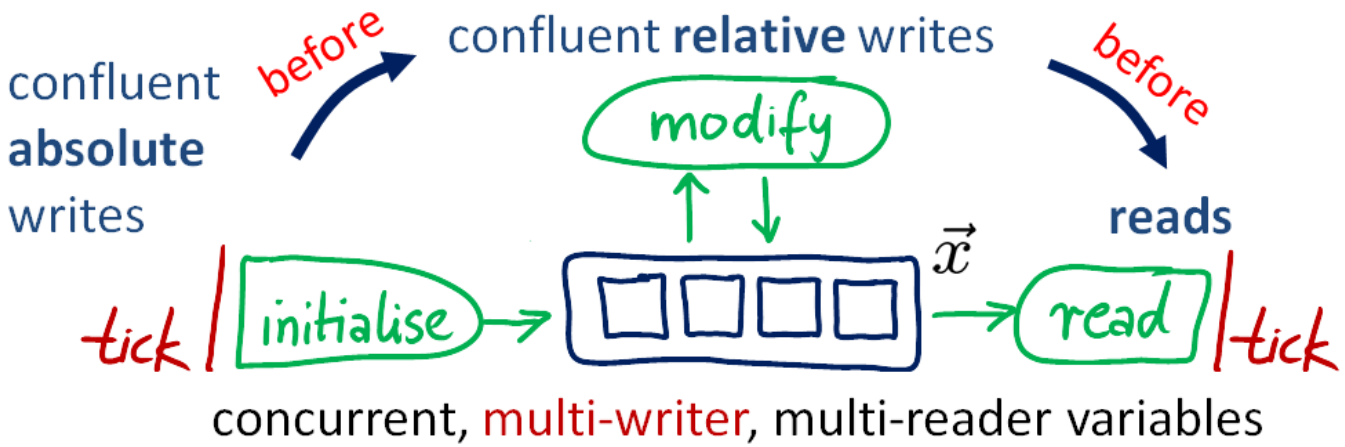

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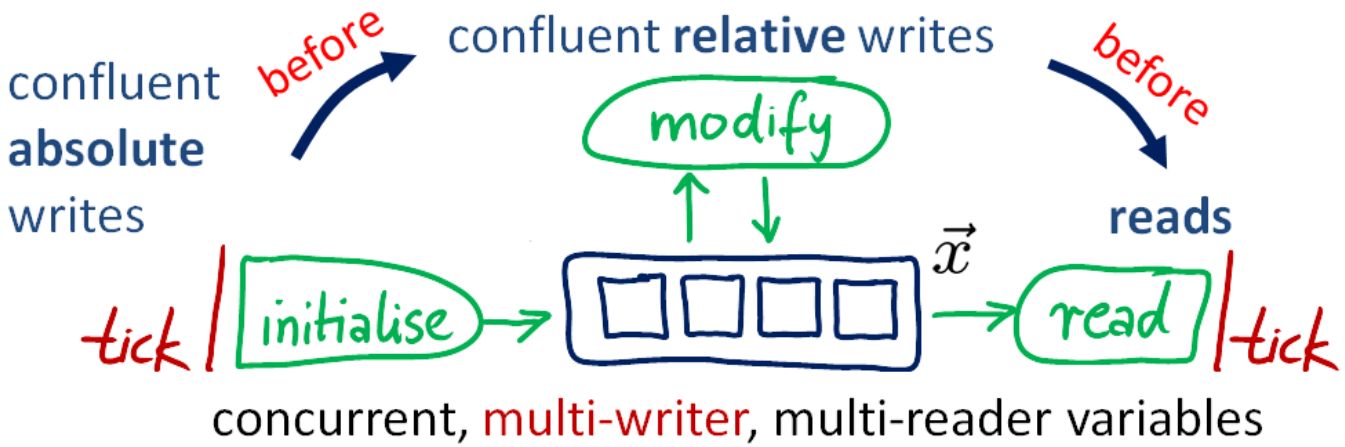

Confluent Statements (per macro tick)

Organizing Concurrent Variable Accesses

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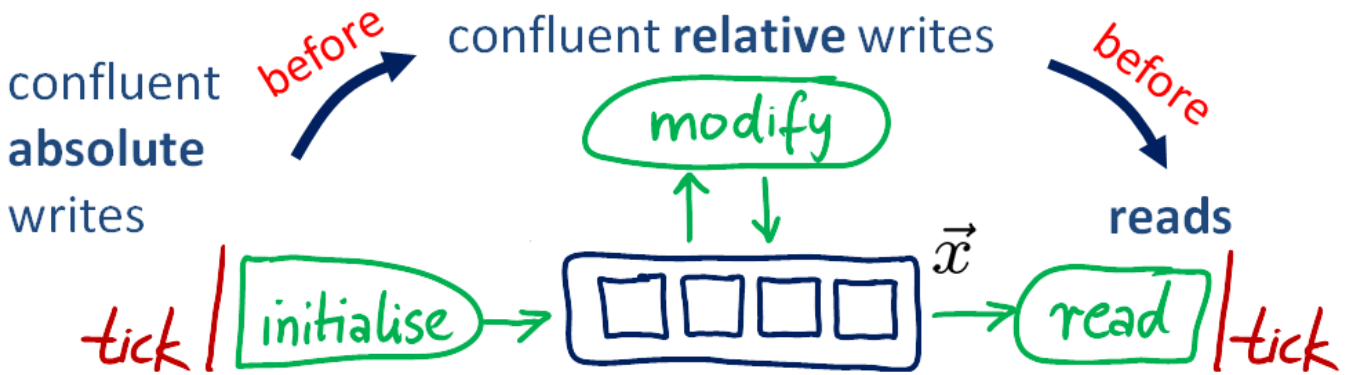

concurrent, multi-writer, multi-reader variables

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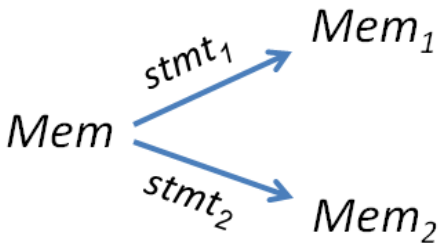

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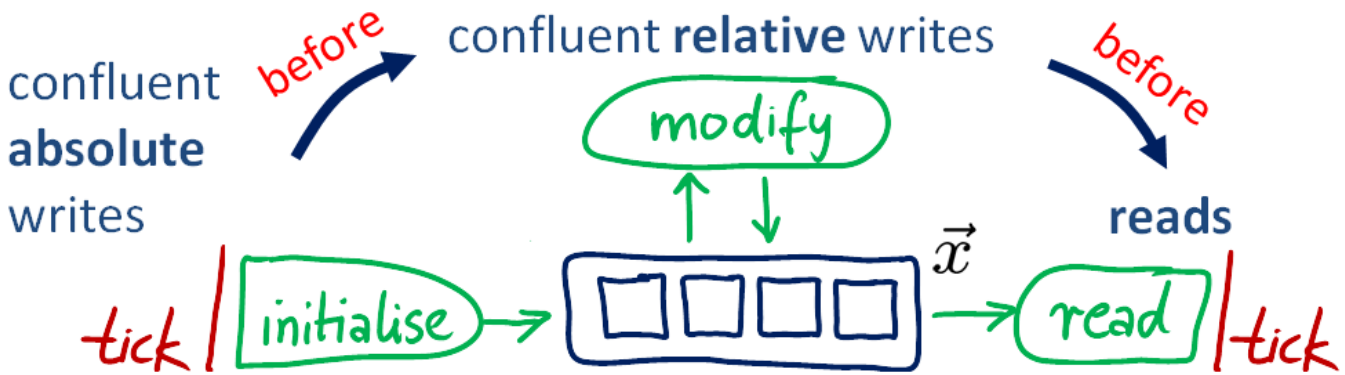

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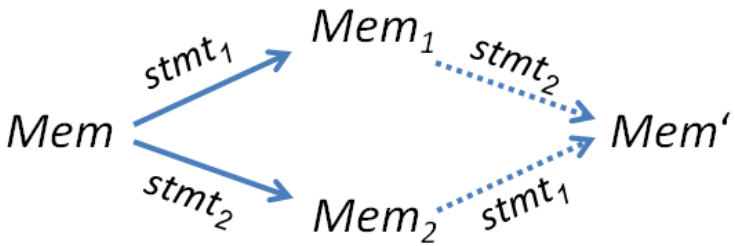

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3. Want to exploit sequentiality as much as possible
   - But what exactly *is* sequentiality?
4. Want to define not only the exact concept of SC, but also a practical strategy to implement it
   - In practice, this requires conservative approximations
   - Compiler must not accept Non-SC programs
   - Compiler may reject SC programs

References

Most of the material here draws from this reference [TECS]:

R. von Hanxleden, M. Mendler, J. Aguado, B. Duderstadt, I. Fuhrmann, C. Motika, S. Mercer, O. O'Brien, and P. Roop.
Sequentially Constructive Concurrency – A Conservative Extension of the Synchronous Model of Computation.
ACM Transactions on Embedded Computing Systems, Special Issue on Applications of Concurrency to System Design, July 2014, 13(4s).
http://rtsys.informatik.uni-kiel.de/~biblio/downloads/papers/tecs14.pdf

Unless otherwise noted, the numberings of definitions, sections etc. refer to this.

There is also an extended version [TR]:

R. von Hanxleden, M. Mendler, J. Aguado, B. Duderstadt, I. Fuhrmann, C. Motika, S. Mercer, O. O'Brien, and P. Roop.
Sequentially Constructive Concurrency – A Conservative Extension of the Synchronous Model of Computation.
Christian-Albrechts-Universität zu Kiel, Department of Computer Science, Technical Report 1308, ISSN 2192-6247, Aug. 2013, 13(4s).
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Overview

The Sequentially Constructive Language (SCL) [Sec. 2.1]

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$$s ::= \quad x = e \mid s;s \mid \textbf{if } (e)\ s\ \textbf{else } s \mid l : s \mid \textbf{goto } l \mid \textbf{fork } s\ \textbf{par } s\ \textbf{join} \mid \textbf{pause}$$

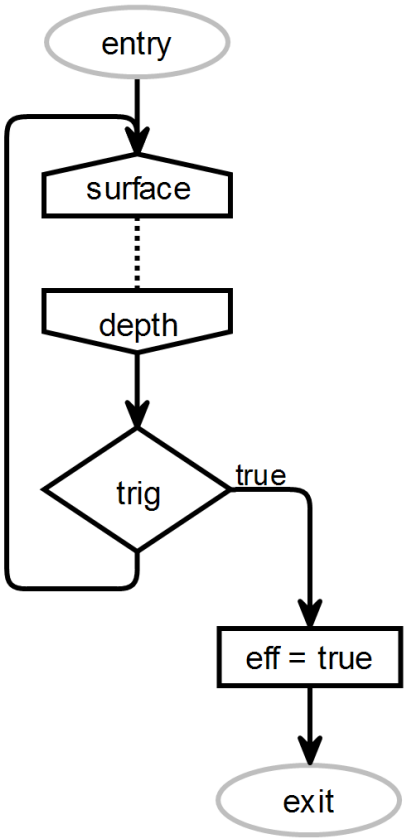
s Statement

x Variable

e Expression

l Program label

The SC Graph (SCG) [Sec. 2.3]



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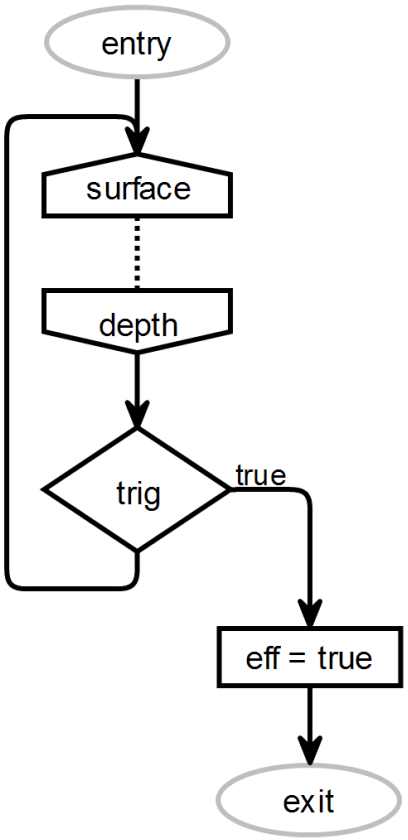

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Internal representation for

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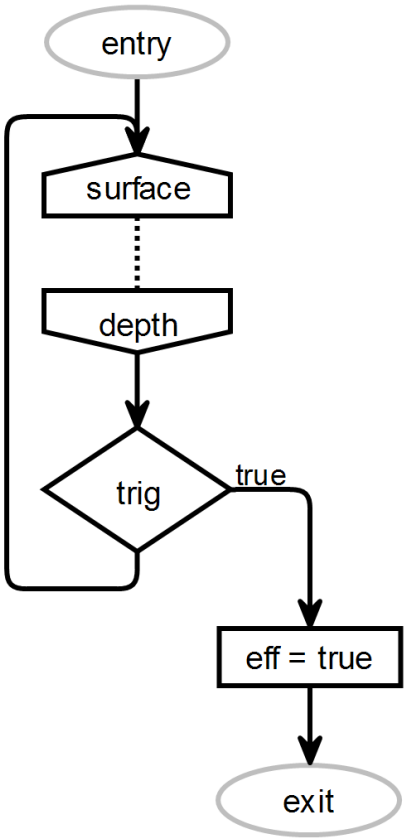

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SC Graph:

Labeled graph $G = (N, E)$

- Nodes N correspond to statements of sequential program
- Edges E reflect sequential execution control flow

Node Types in the SCG

Node $n \in N$ has statement type $n.st$

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- $n.st \in$
  $\{\text{entry}, \text{exit}, \text{goto}, x = ex, \text{if}\,(ex), \text{fork}, \text{join}, \text{surf}, \text{depth}\}$
- x: variable, ex: expression.

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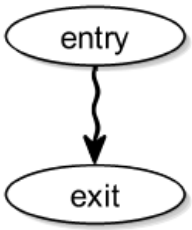
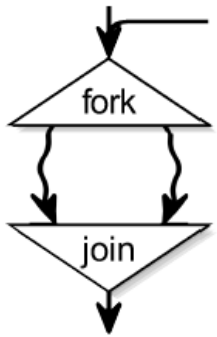
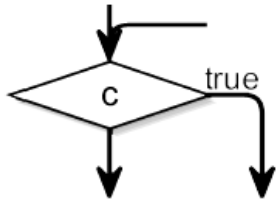
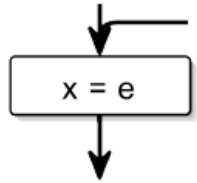
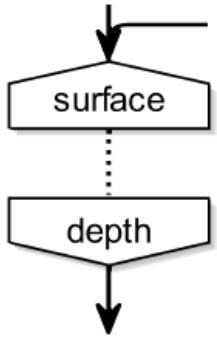
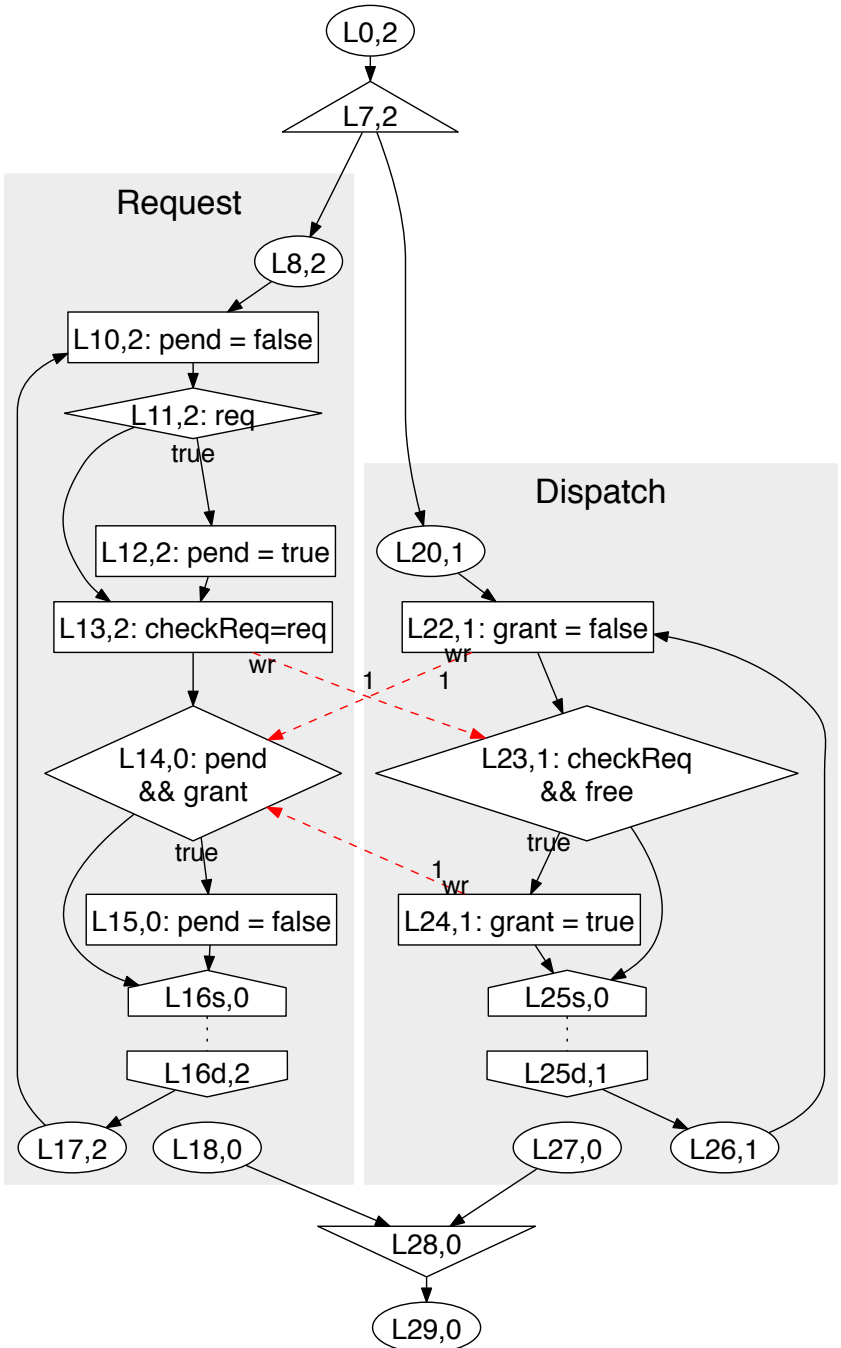
Mapping SCL & SCG

	Thread (Region)	Concurrency (Superstate)	Conditional (Trigger)	Assignment (Effect)	Delay (State)
SCG					
SCL	t	fork t_1 par t_2 join	if (c) s_1 else s_2	$x = e$	pause

Plus ";" (Sequence) and "goto" to specify sequential successors (solid edges)

SCL & SCG – The Control Example

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- For each thread t, define $sts(t)$ as the set of statement nodes $n \in N$ such that $th(n) = t$

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Threads in Control Example

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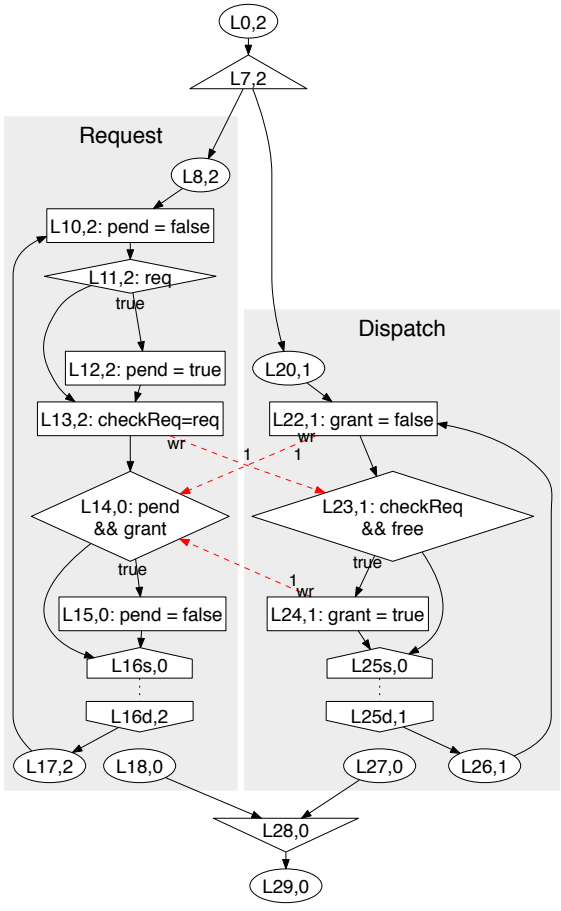

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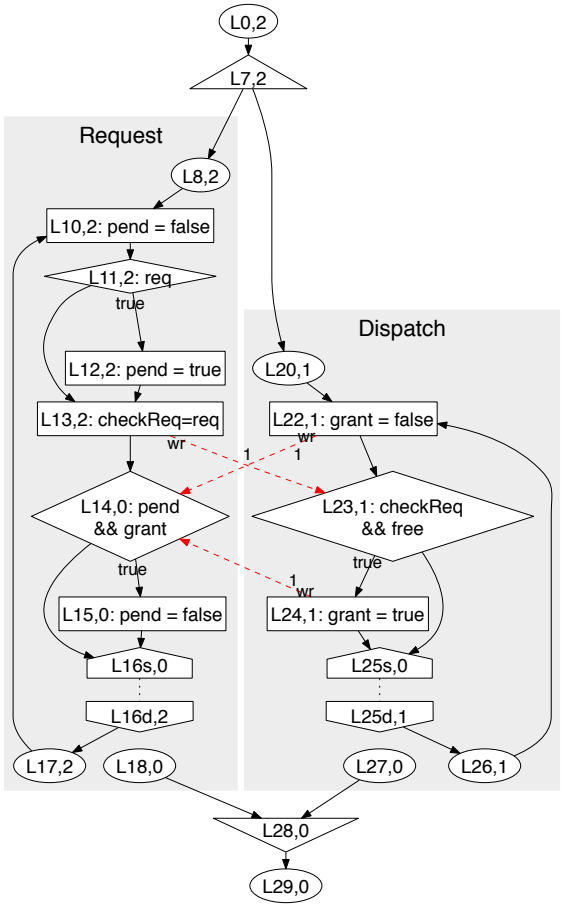

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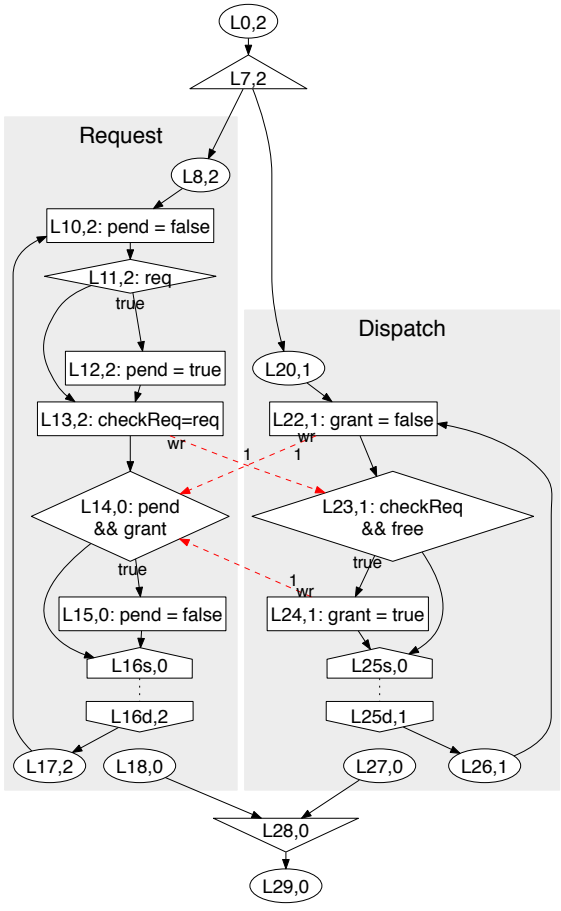

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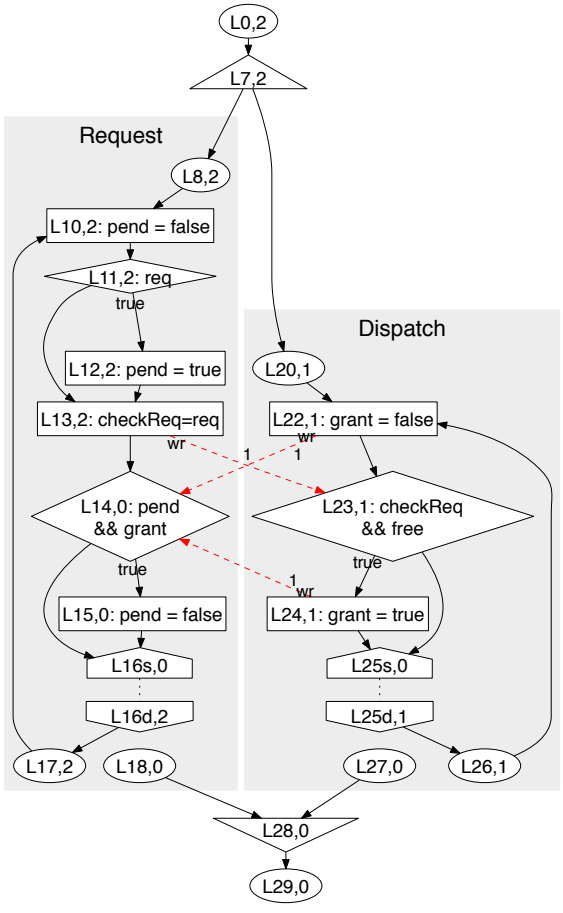

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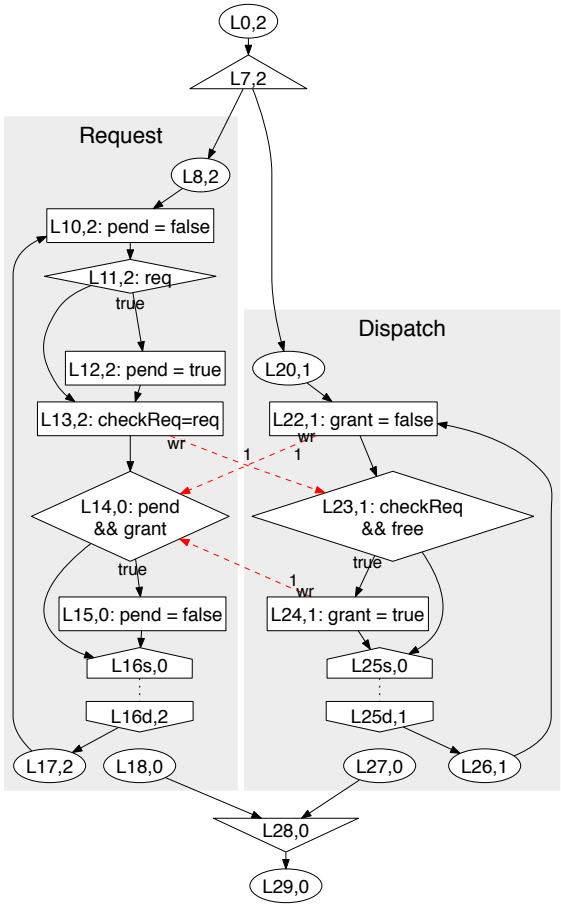

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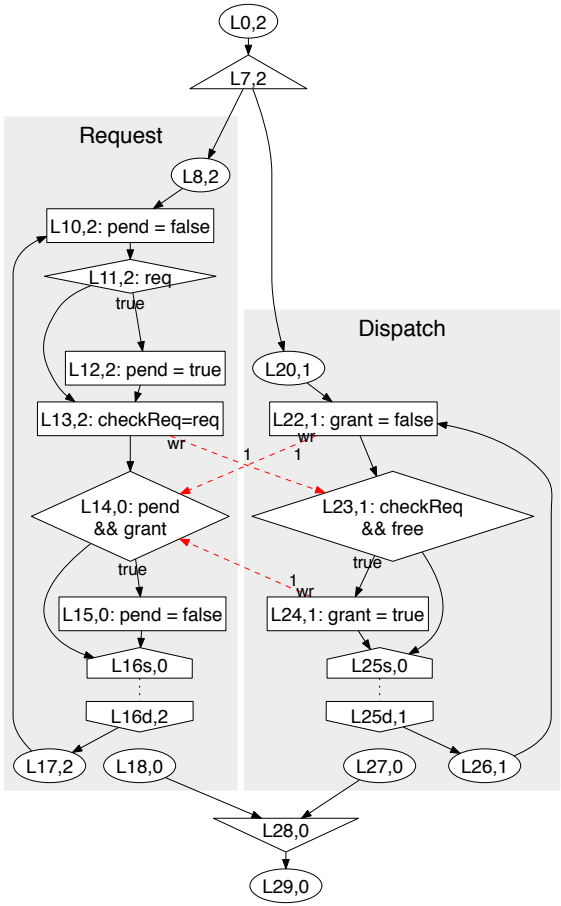

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Let t, t_1, t_2 be threads in T

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Concurrency and Subordination in Control-Program

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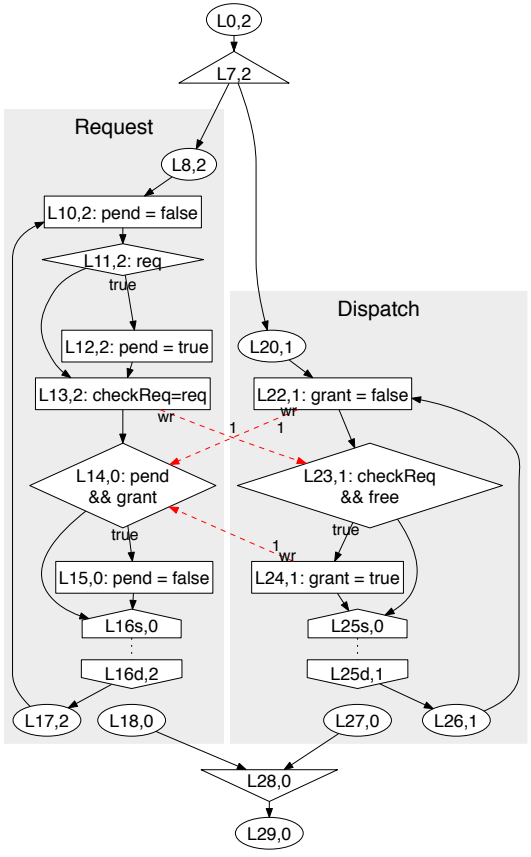

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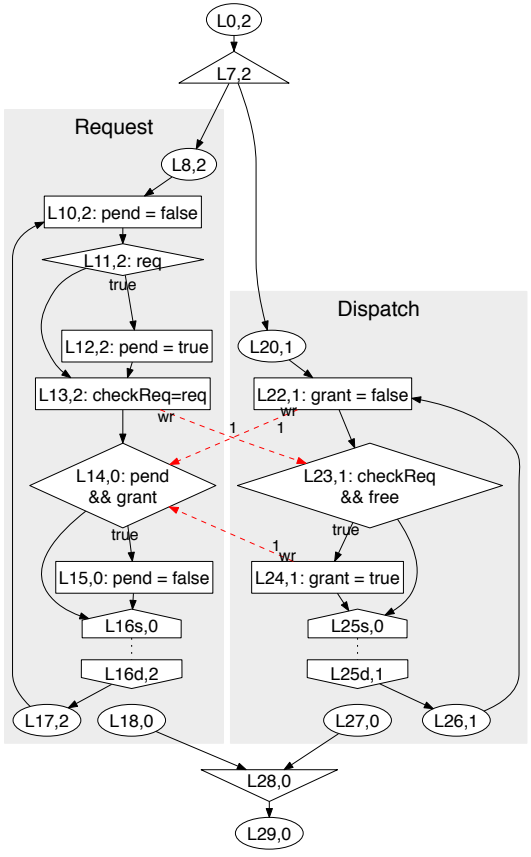

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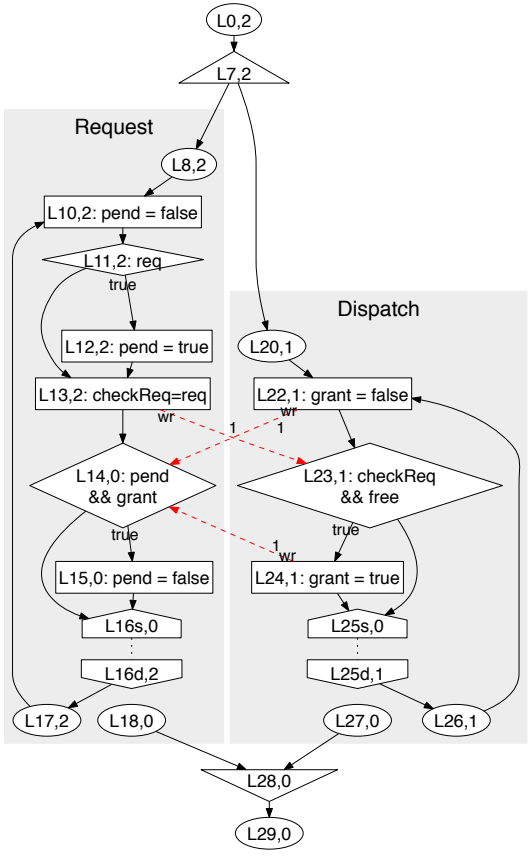

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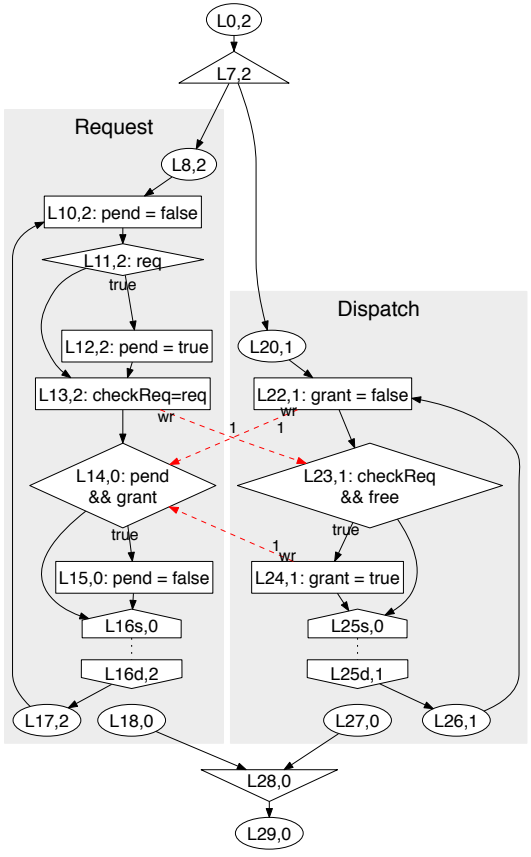

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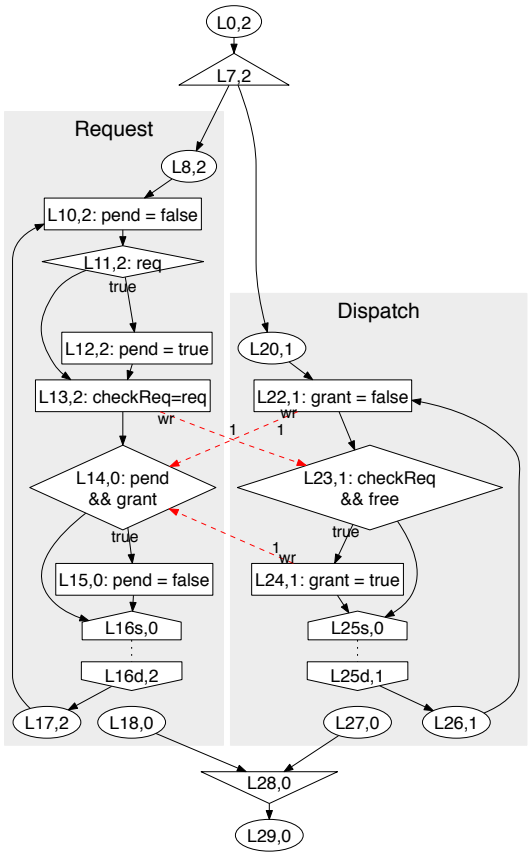

- *Root* $\prec$ *Request* and *Root* $\prec$ *Dispatch*
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Note: Concurrency on threads, in contrast to concurrency on node instances, is purely static and can be checked with a simple, syntactic analysis of the program structure.

Thread Trees [TR, Sec. 3.7]

A Thread Tree illustrates the static thread relationships.

- Contains subset of SCG nodes:
  1. Entry nodes, labeled with names of their threads
  2. Fork nodes, attached to the entry nodes of their threads
- Similar to the AND/OR tree of Statecharts

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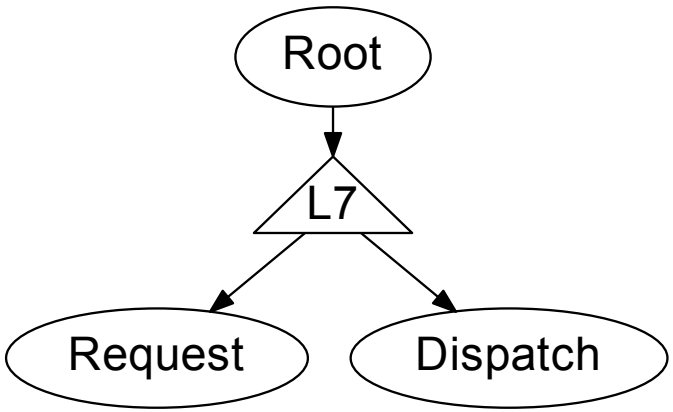

Thread Trees – The Reinc2 Example

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2  output int x, y;
3  {
4   loop:
5    fork { // Thread T1
6      x = 1; }
7    par { // Thread T2
8      fork { // Thread T21
9        y = 1; }
10     par { // Thread T22
11       pause;
12       y = 2; }
13     join;
14     fork { // Thread T23
15       y = 3; }
16     par { // Thread T24
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19 join;
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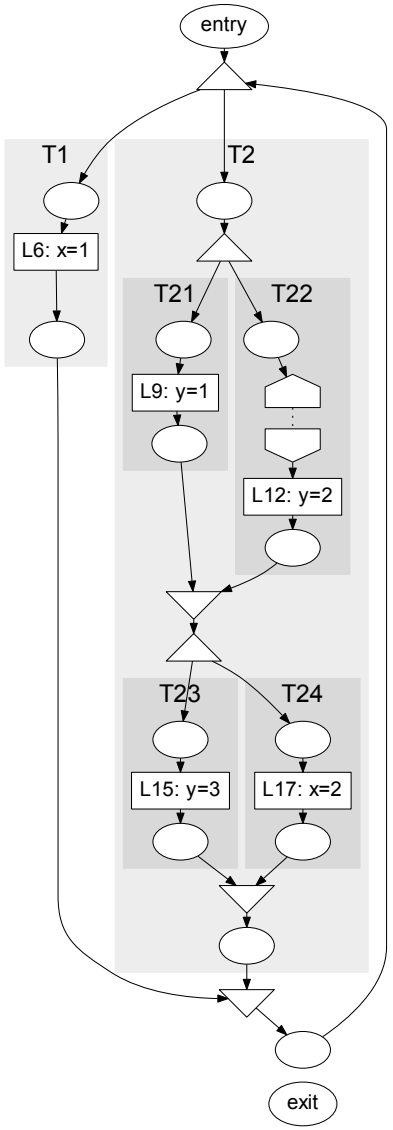

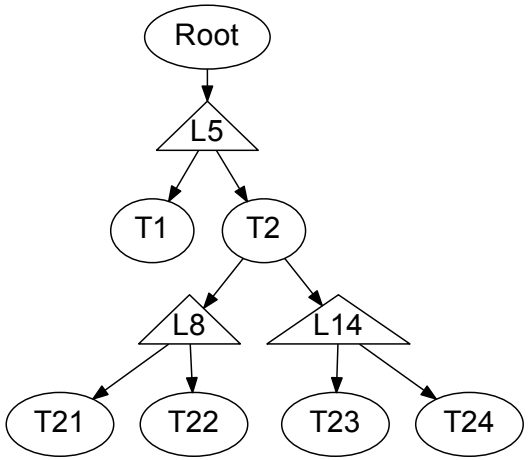

Alternative definition for static thread concurrency:

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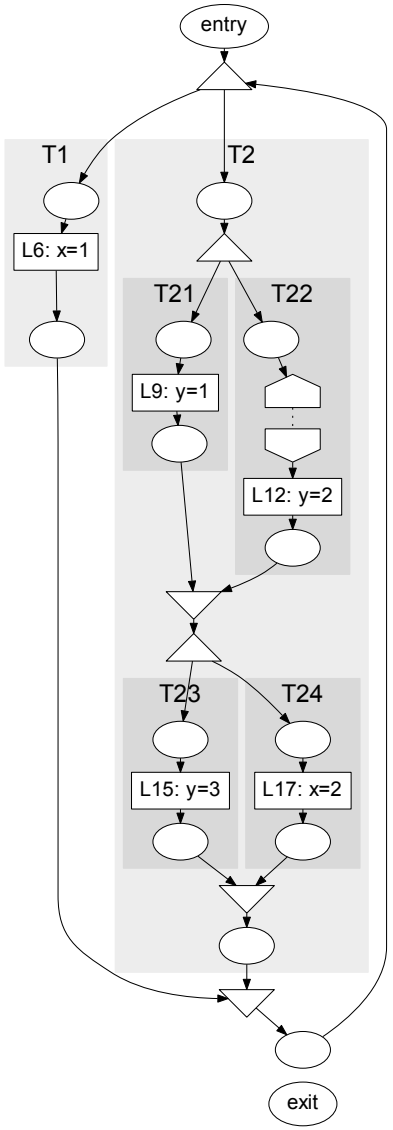

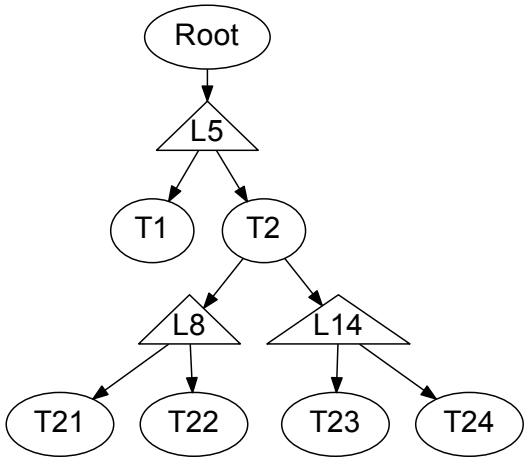

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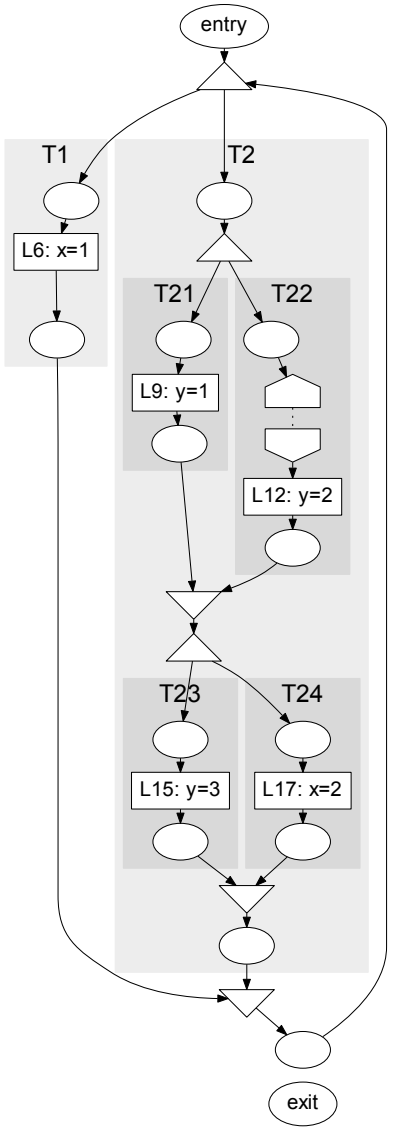

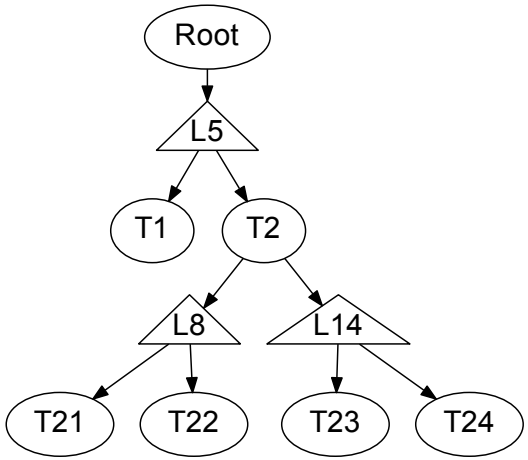

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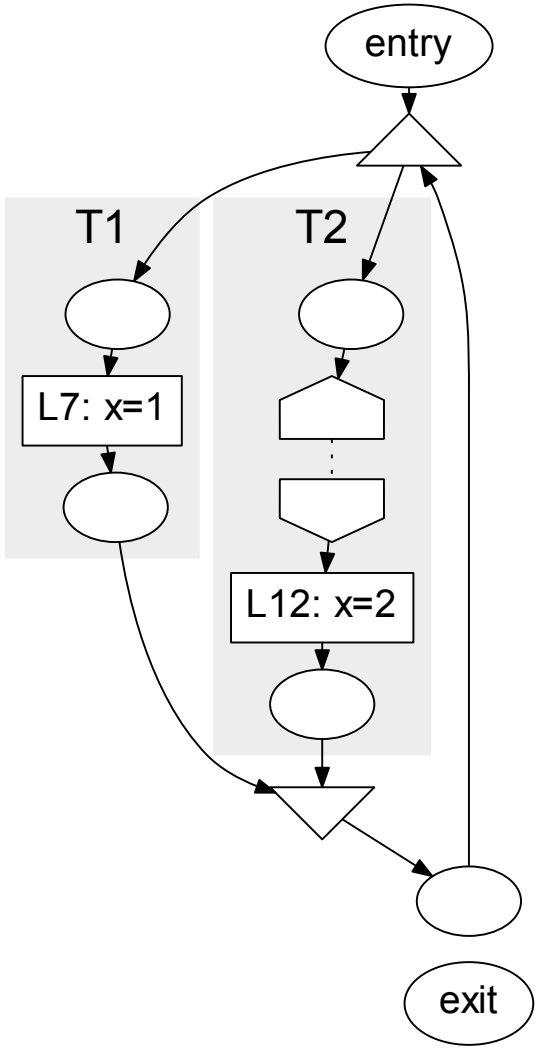

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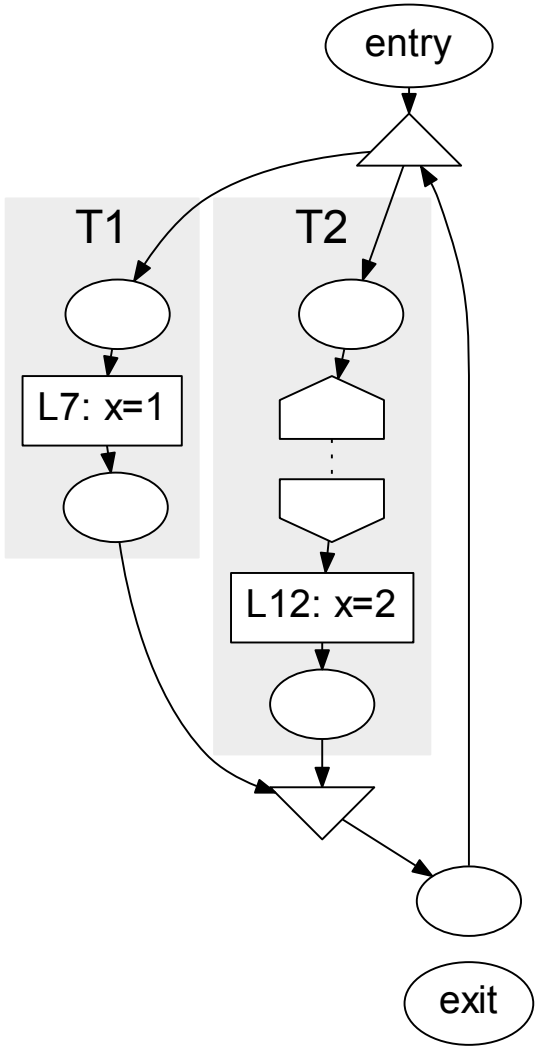

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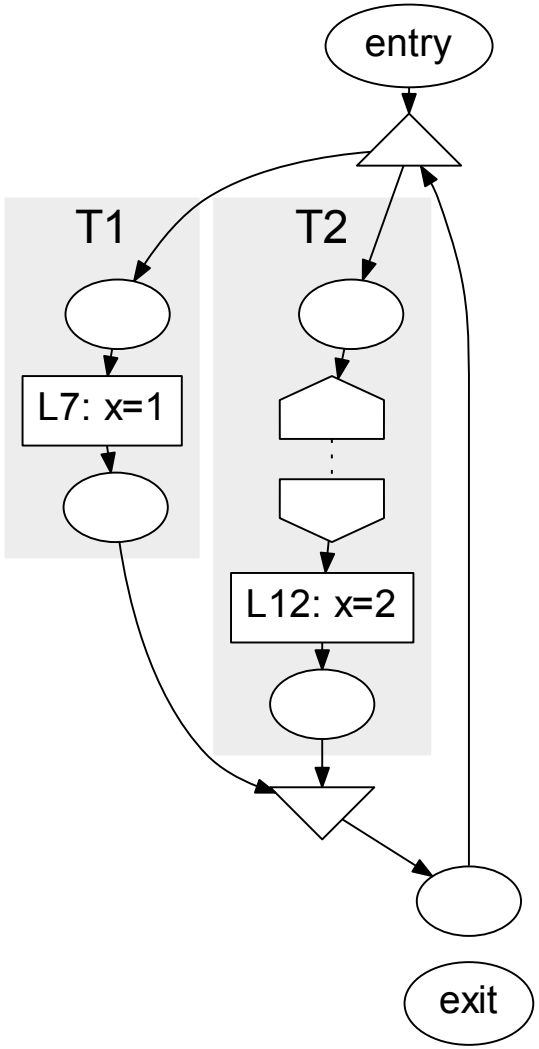

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Observations:

- T2 exhibits thread reincarnation

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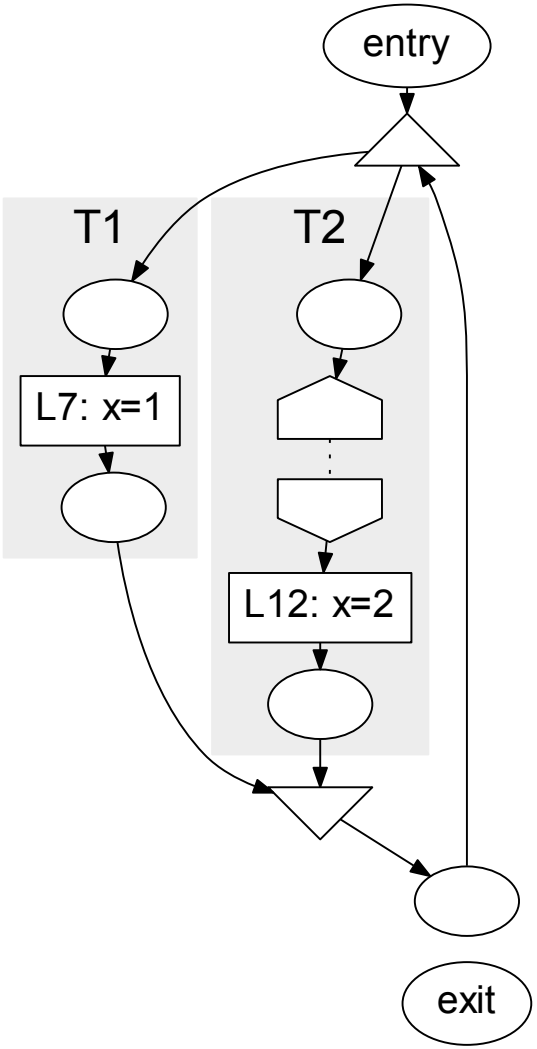

Are interested in run-time concurrency, *i. e.*, whether ordering is up to discretion of a scheduler.

Observations:

- T2 exhibits thread reincarnation
- Assignments to x are both executed in the same tick, yet are sequentialized

Thread Reincarnation – The Reinc Example

```
1  module Reinc
2  output int x, y;
3  {
4  loop:
5   fork {
6     // Thread T1
7     x = 1;
8   }
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10    // Thread T2
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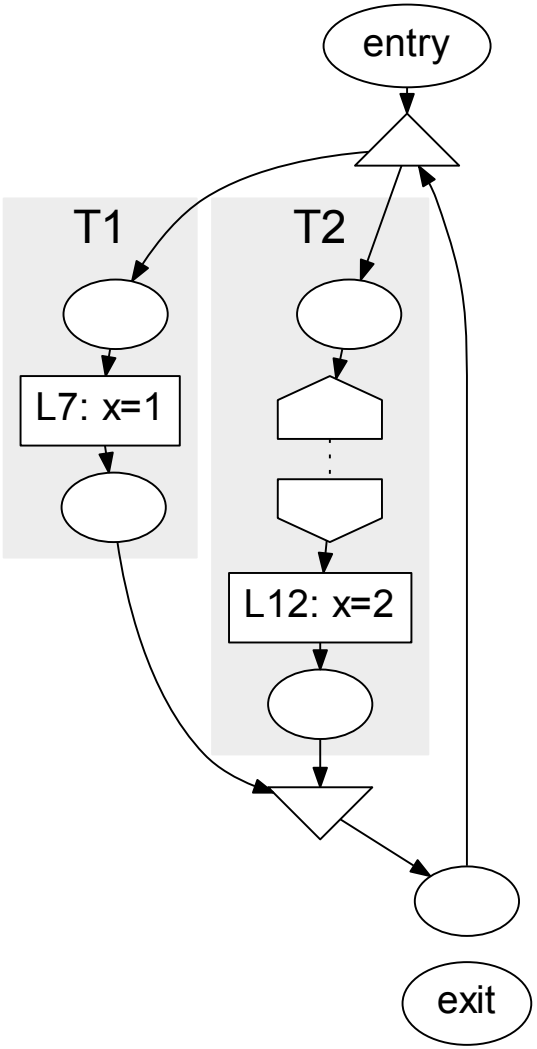

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- Thus, **static thread concurrency not sufficient to capture run-time concurrency**!

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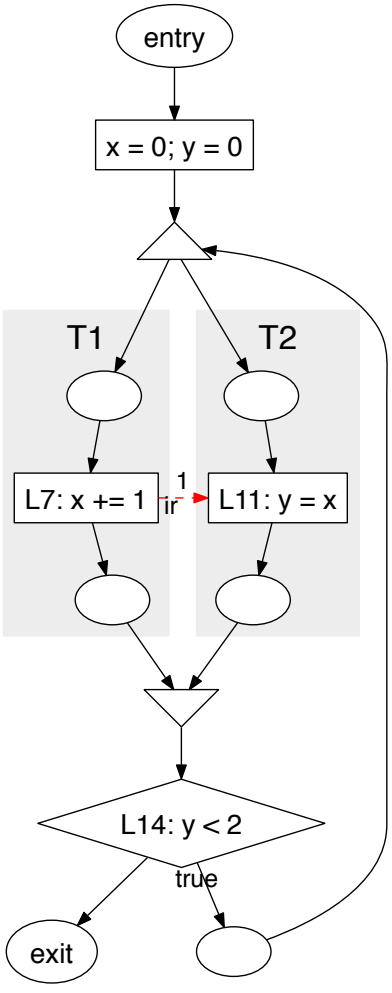


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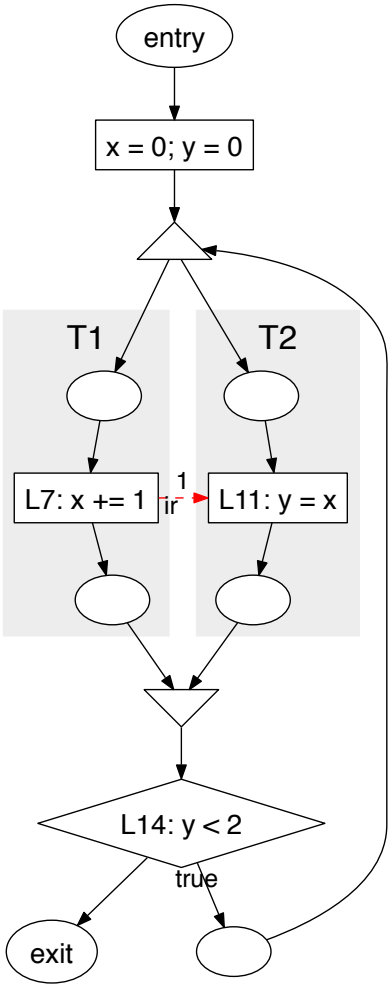


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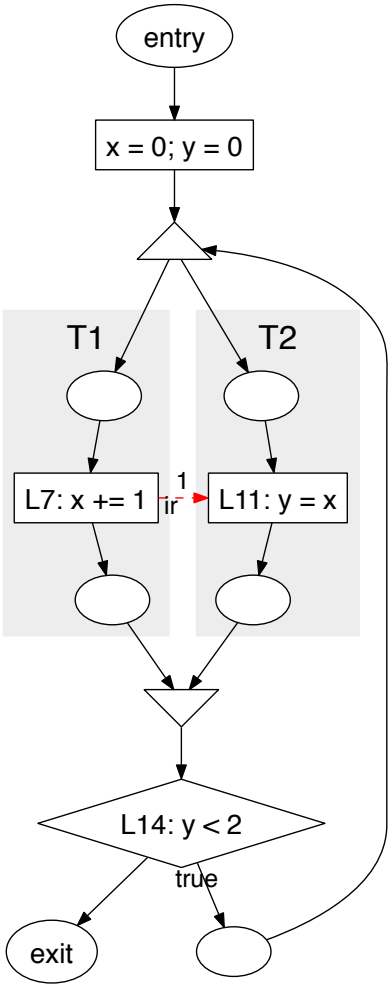


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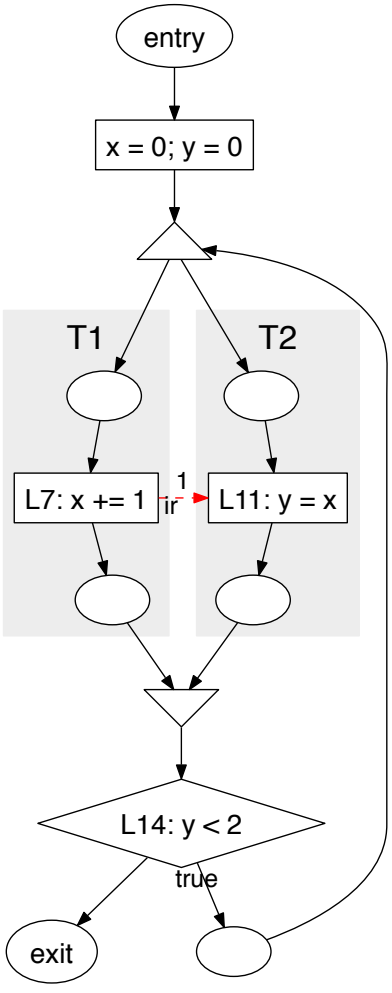


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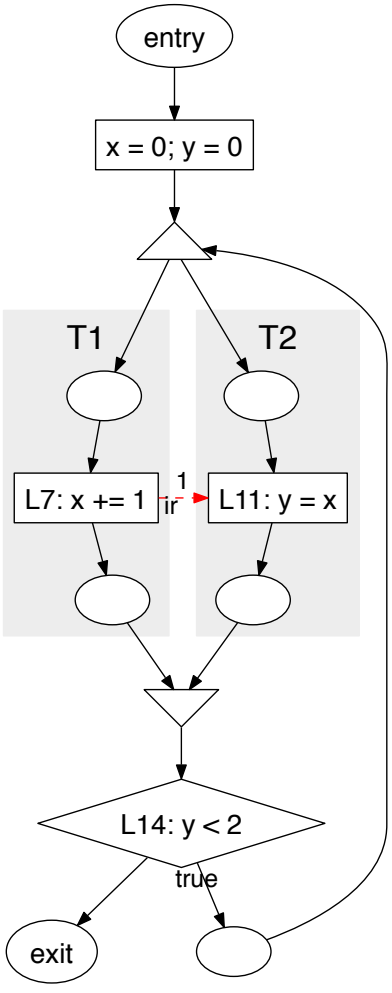


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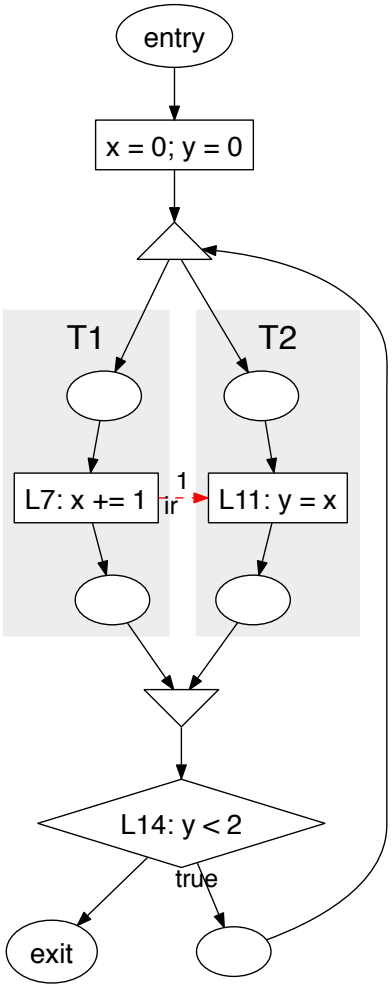


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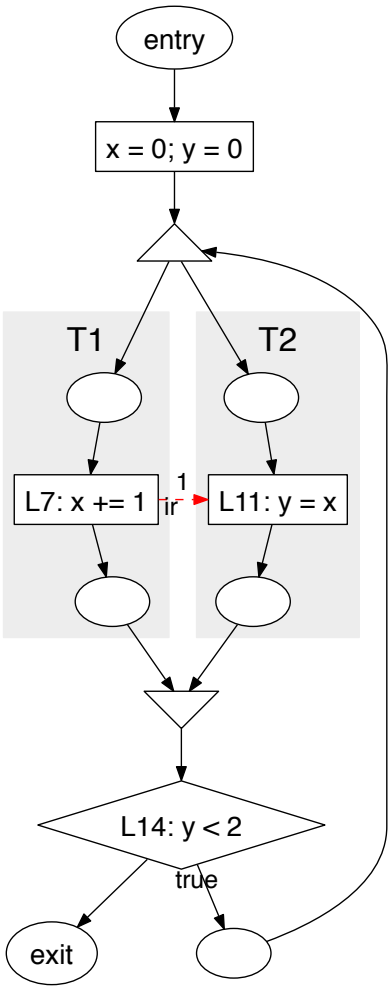
Not enough to impose an order on the program statements
$\Rightarrow$ Need to distinguish statement instances

Statement Reincarnation II

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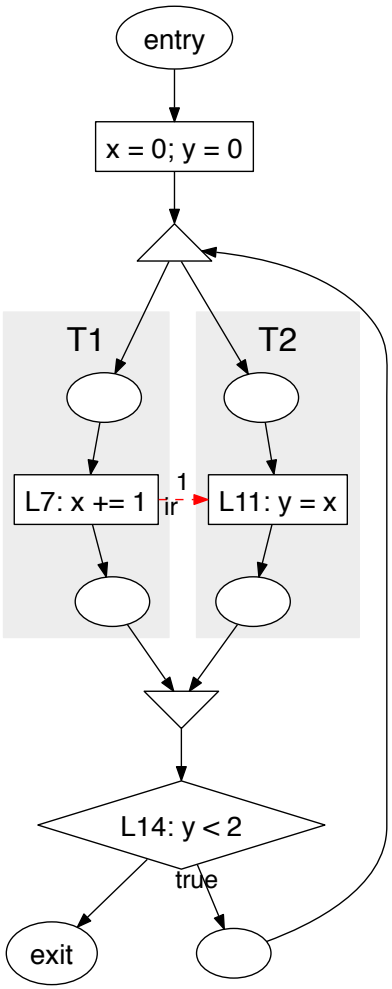


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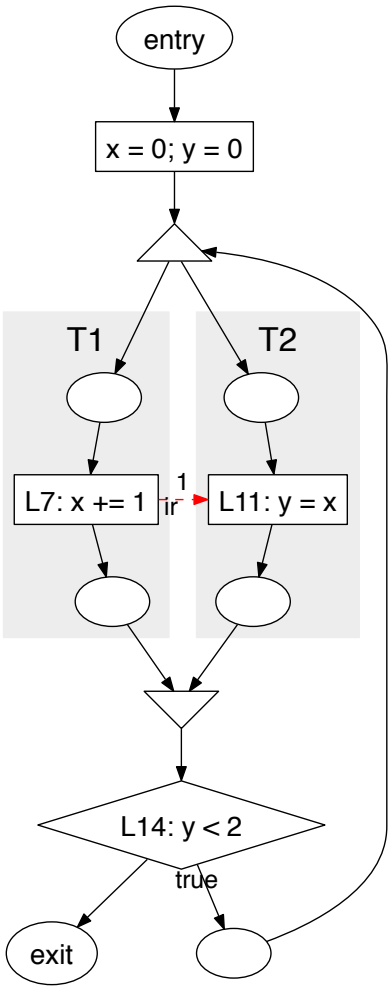


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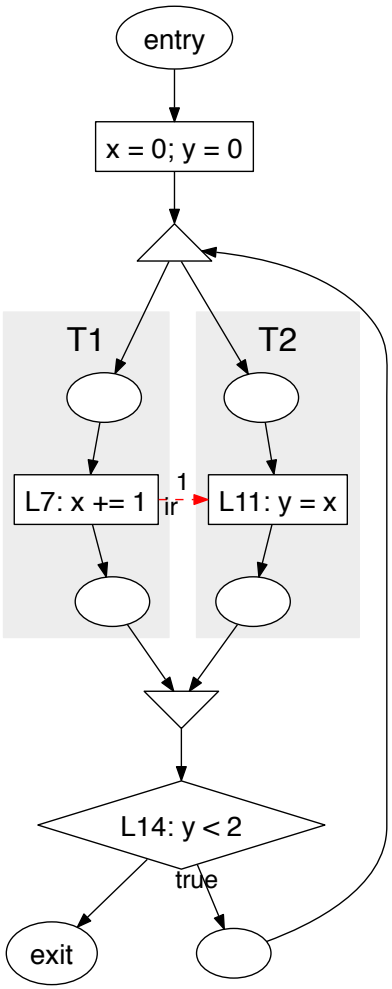


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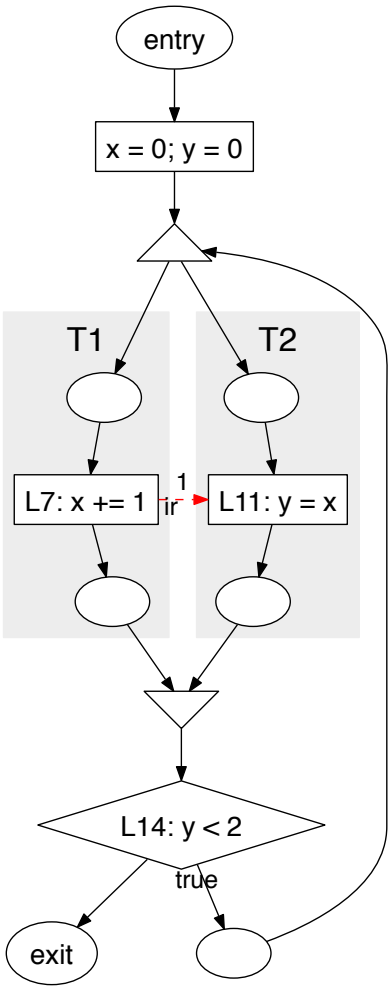


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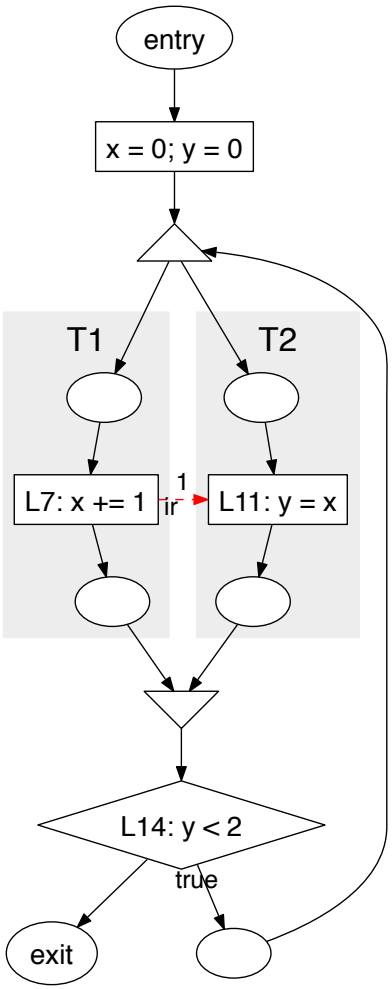


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Macroticks [Def. 2.3 + 2.4]

- Given: SCG $G = (N, E)$
- (Macro) tick R, of length $len(R) \in \mathbb{N}_{\geq 1}$:
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Given: macro tick R, index $1 \leq i \leq len(R)$, node $n \in N$

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Overview

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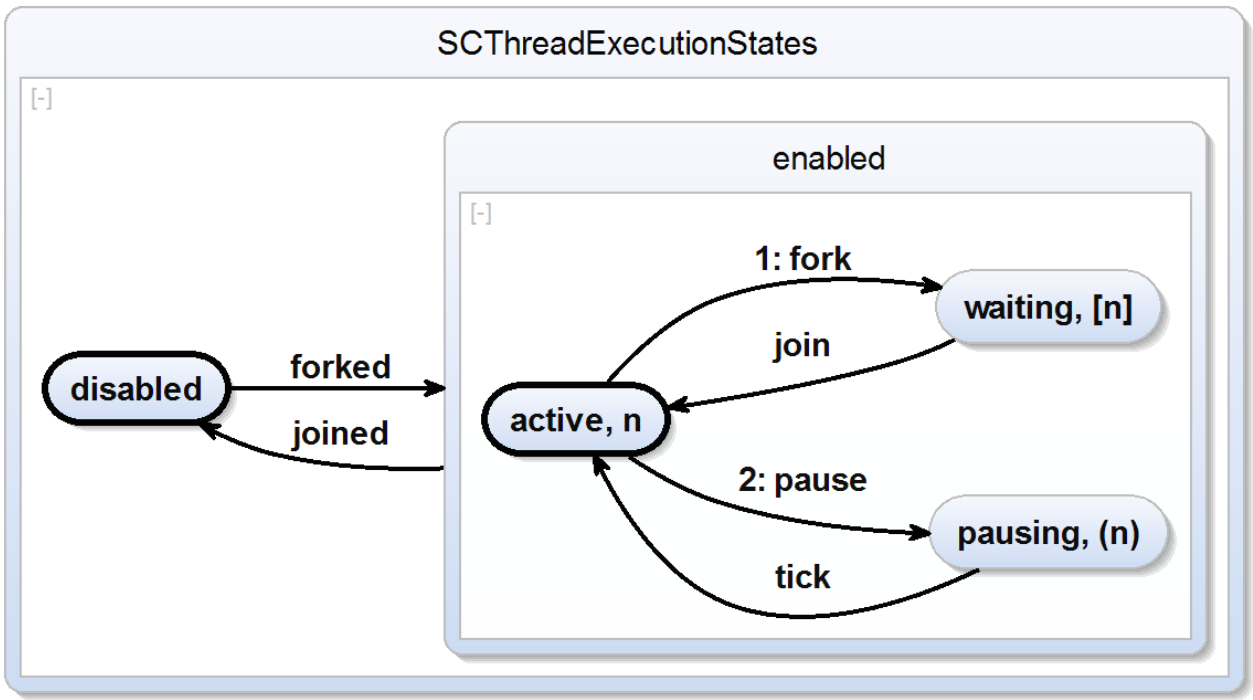

In a trace (see later slide), round/square/no parentheses around $n = c.node$ denote $c.status$, for enabled continuations c

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A configuration is called valid if C is valid

```
1  module Control
2  input bool free, req;
3  output bool grant, pend;
4  {
5    bool checkReq;
6
7    fork {
8      // Thread Request
9      Request entry:
10     pend = false;
11     if (req)
12       pend = true;
13     checkReq = req;
14     if (pend && grant)
15       pend = false;
16     pause;
17     goto Request entry;
18   }
19   par {
20     // Thread Dispatch
21     Dispatch entry:
22     grant = false;
23     if (checkReq && free)
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25     pause;
26     goto Dispatch entry;
27   }
28   join;
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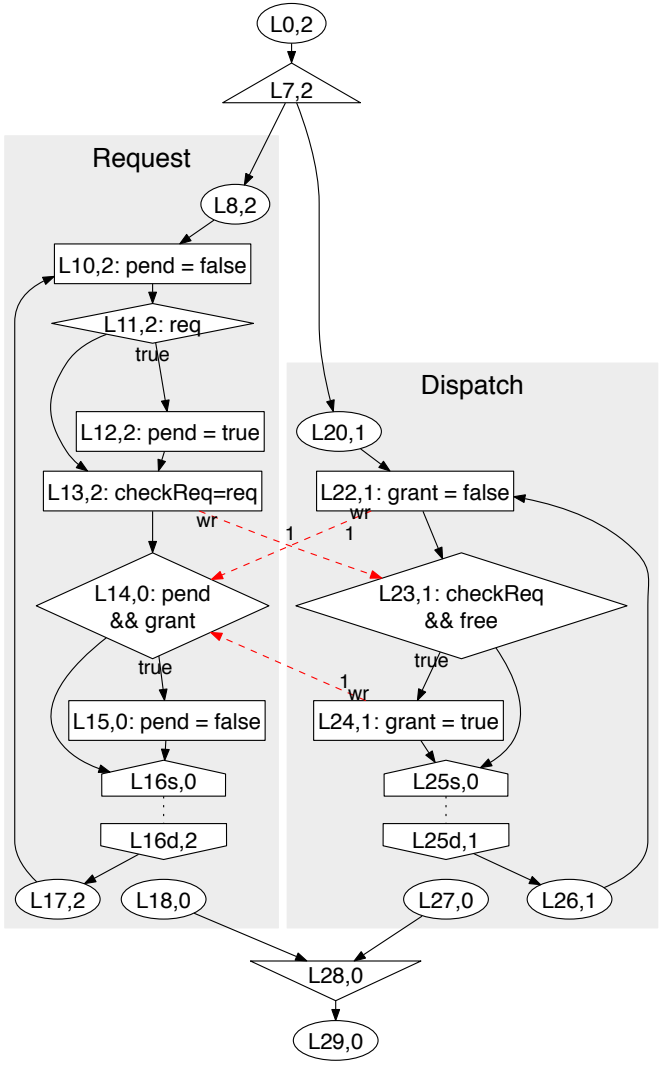

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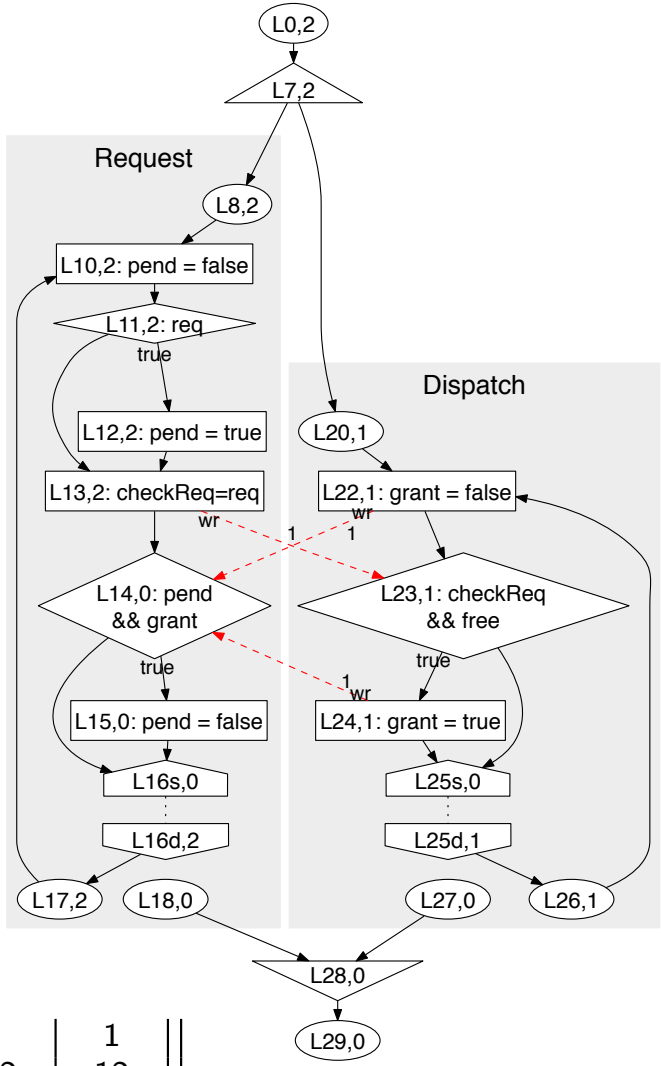
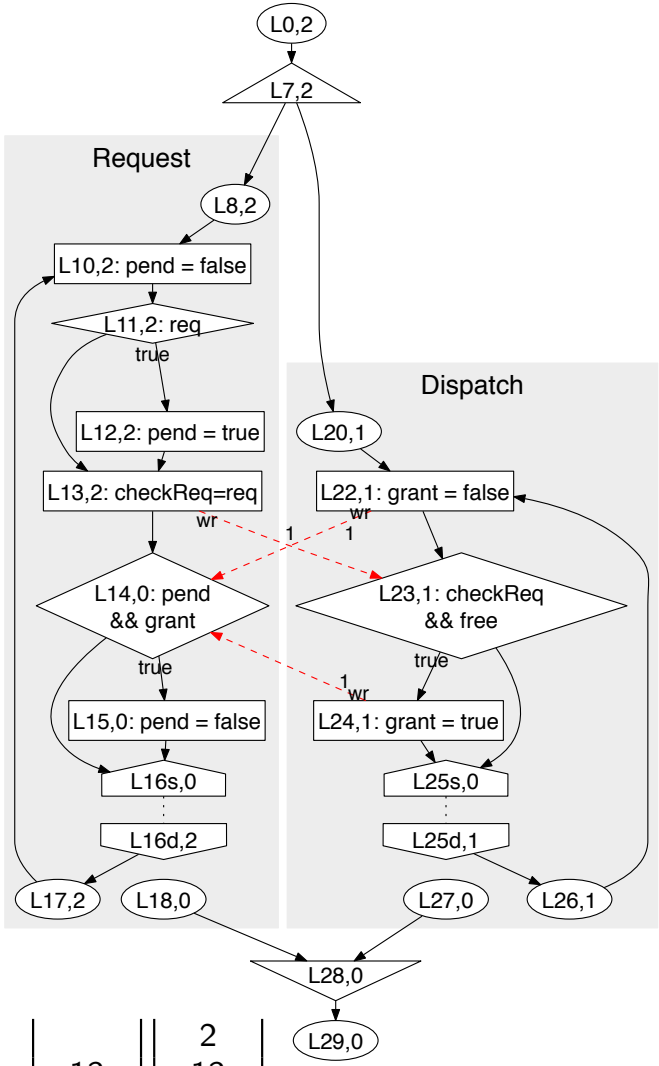


Macro tick	*a*	1											1
Micro tick	*i*	1	2	3	4	5	6	7	8	9	10	11	12	12
Input vars	free	**t**												*t*
	req	**f**												*f*
Output vars	grant	⊥								*f*				**f**
	pend	⊥				*f*								**f**
Local var	checkReq	⊥						*f*						*f*
Continuations	C_{Root}	L0	L7	[L28]										[L28]
	C_{Request}	⊥		L8	L10	L11	L13	L14	L14	L14	L14	L14	L16s	(L16s)
	C_{Dispatch}	⊥		L20	L20	L20	L20	L20	L22	L23	L25s	(L25s)	(L25s)	(L25s)
Scheduled nodes R_i^a		L0	L7	L8	L10	L11	L13	L20	L22	L23	L25s	L14	L16s	

```
1  module Control
2  input bool free, req;
3  output bool grant, pend;
4  {
5    bool checkReq;
6
7    fork {
8      // Thread Request
9      Request entry:
10     pend = false;
11     if (req)
12       pend = true;
13     checkReq = req;
14     if (pend && grant)
15       pend = false;
16     pause;
17     goto Request entry;
18   }
19   par {
20     // Thread Dispatch
21     Dispatch entry:
22     grant = false;
23     if (checkReq && free)
24       grant = true;
25     pause;
26     goto Dispatch entry;
27   }
28   join;
29 }
```



Macro tick	*a*	2													2
Micro tick	*i*	1	2	3	4	5	6	7	8	9	10	11	12	13	13
Input vars	free	**t**													*t*
	req	**t**													*t*
Output vars	grant	*f*							*f*		*t*				**t**
	pend	*f*		*f*		*t*								*f*	**f**
Local var	checkReq	*f*					*t*								*t*
Continuations	C_{Root}	[L28]													[L28]
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	C_{Dispatch}	L25d	L25d	L25d	L25d	L25d	L25d	L22	L23	L24	L25s	(L25s)	(L25s)	(L25s)	(L25s)
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2. Do so in an interleaving fashion

Micro Steps I

Micro step: transition $(C_{cur}, M_{cur}) \xrightarrow{c}_{\mu s} (C_{nxt}, M_{nxt})$ between two micro ticks

- (C_{cur}, M_{cur}): current configuration
- c: continuation selected for execution
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The free schedule is permitted to pick any one of the $\prec$-maximal continuations $c \in C_{cur}$ with $c.status = \text{active}$ and execute it in the current memory M_{cur}

Micro Steps II

(Recall:) Micro step: transition $(C_{cur}, M_{cur}) \xrightarrow{c}_{\mu s} (C_{nxt}, M_{nxt})$

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- Actions μM and μC (made precise in paper) depend on the statement $c.node.st$ to be executed
- (C_{nxt}, M_{nxt}) uniquely determined by c, thus may write $(C_{nxt}, M_{nxt}) = c(C_{cur}, M_{cur})$

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Quiescent configuration (C, M):

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- Scheduler can perform a global clock step

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Global clock step $V_I : (C_{cur}, M_{cur}) \rightarrow_{tick} (C_{nxt}, M_{nxt})$

- Transition between last micro tick of the current macro tick to first micro tick of the subsequent macro tick
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- V_I is external input
- All pausing continuations of C advance from their surf node to the associated depth node:

$$\begin{aligned} C_{nxt} \quad = \quad & \{c[\text{active} :: tick(n)] \mid c[\text{pausing} :: n] \in C_{cur}\} \cup \\ & \{c[\text{waiting} :: n] \mid c[\text{waiting} :: n] \in C_{cur}\} \end{aligned}$$

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Formally,

$$M_{nxt}(x) = \begin{cases} v_i, & \text{if } x = x_i \in I, \\ M_{cur}(x), & \text{if } x \notin I. \end{cases}$$

Macro Ticks

Scheduler runs through sequence

$$(C_0^a, M_0^a) \xrightarrow{c_1^a}_{\mu s} (C_1^a, M_1^a) \xrightarrow{c_2^a}_{\mu s} \cdots \xrightarrow{c_{k(a)}^a}_{\mu s} (C_{k(a)}^a, M_{k(a)}^a) \tag{1}$$

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R^a: sequence of statement nodes executed during a

- $len(R^a) = k(a)$ is length of a
- R^a is function mapping each micro tick index $1 \leq j \leq k(a)$ to node $R^a(j) = c_j^a.node$ executed at index j

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Trace: externally visible output values at each macro tick R [TR, Sec. 3.9]

Determinacy

Recall:

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Active and Pausing Continuations are Concurrent [TR, Prop. 2]

Given:

- (C, M), reachable (micro or macro tick) configuration
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Then:

- $c_1.node \neq c_2.node$
- $th(c_1.node) \mid\mid th(c_2.node)$
- No instantaneous sequential path from $c_1.node$ to $c_2.node$ or vice versa

(Proof: see [TR])

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Recall: Want to exploit sequentiality as much as possible

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Recall: Static concurrency $\not\Rightarrow$ run-time concurrency

- Consider Reinc example
- Thus, can ignore some statically concurrent data dependencies

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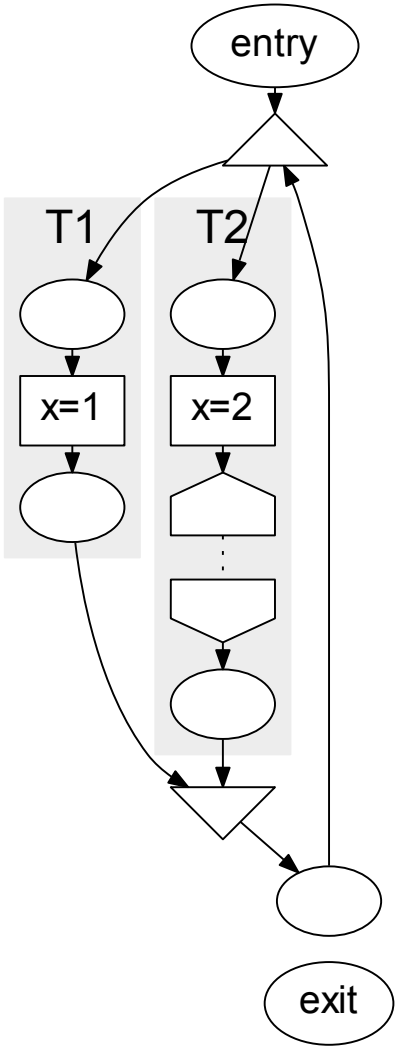

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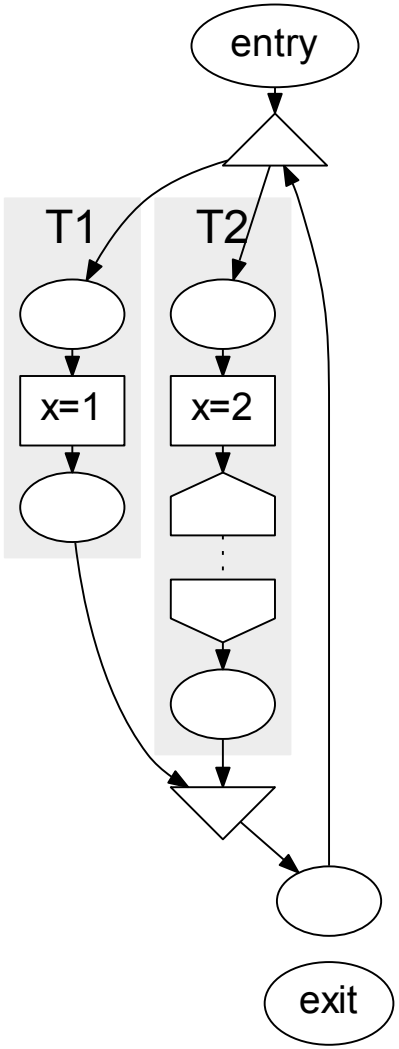

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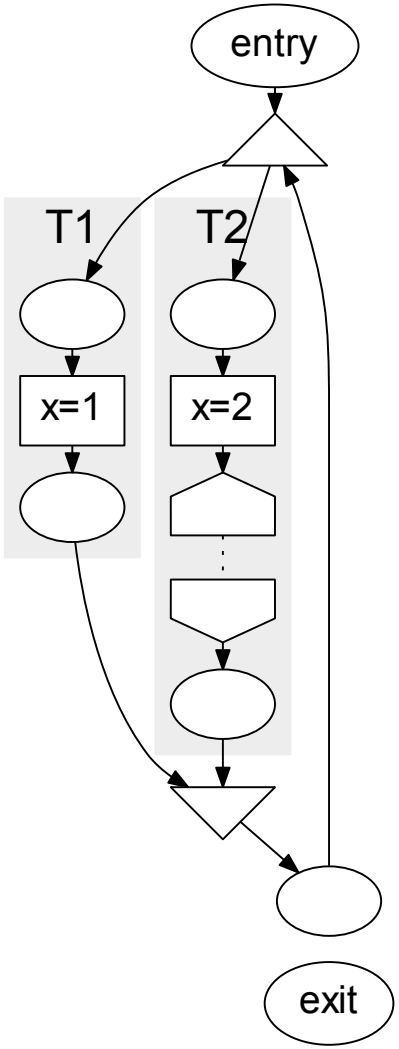

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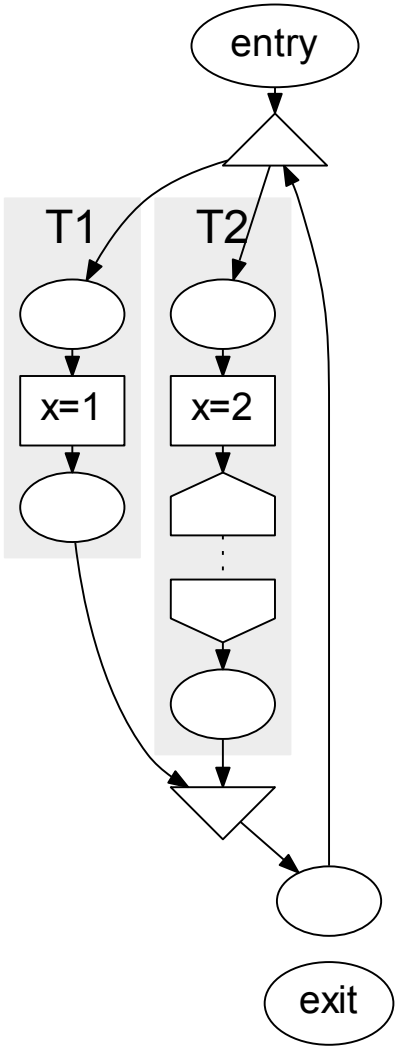

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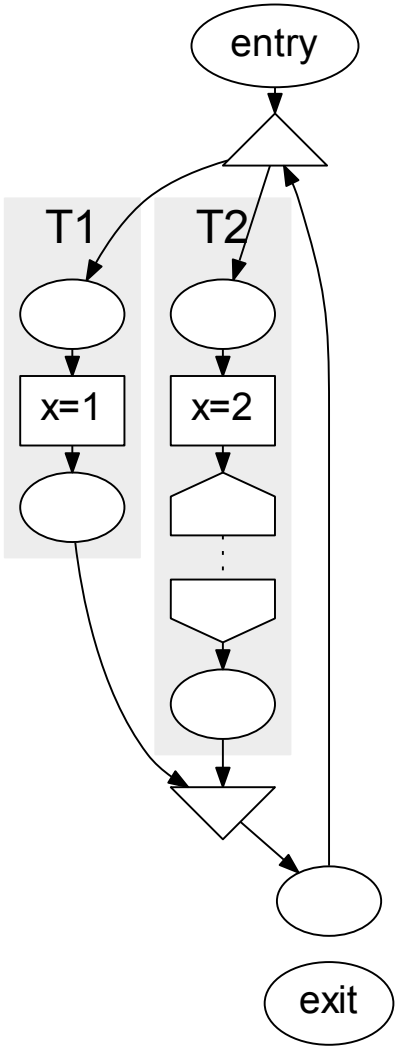

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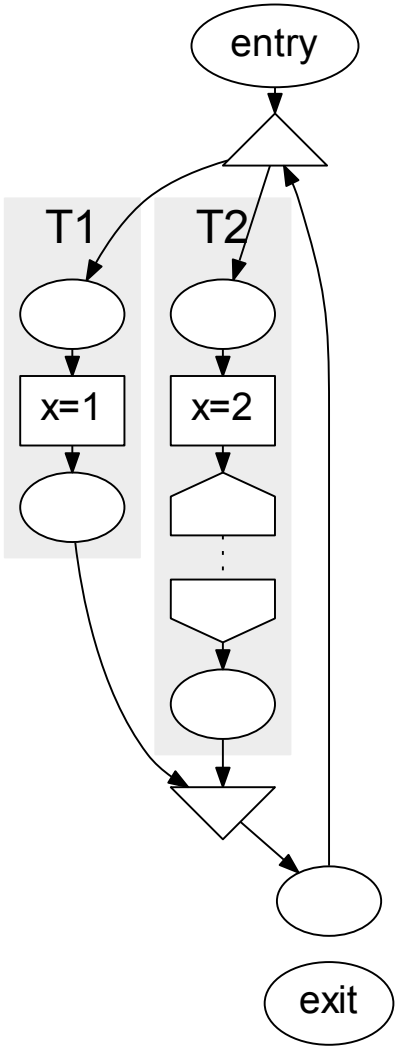
Thus, concurrency and (static) sequentiality are not **mutually exclusive, but orthogonal**!
However, (instantaneous) *run-time* sequentiality (on node *instances*) does exclude run-time concurrency



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- Like the synchronous MoC, the SC MoC ensures macro-tick determinacy by inducing certain scheduling constraints on variable accesses
- **Unlike** the synchronous MoC, the SC MoC tries to take **maximal advantage of the execution order already expressed by the programmer** through sequential commands
- A scheduler can only affect the order of variable accesses through **concurrent** threads

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Similarly, threads are not concurrent with parent thread

- Because of path ordering $\prec$, a parent thread is always suspended when a child thread is in operation
- Thus, not up to scheduler to decide between parent and child thread
- No race conditions between variable accesses performed by parent and child threads; no source of non-determinacy

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In the following, will define such a restriction:

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In the following, will define such a restriction:
the SC-admissible schedules

Guideline for SC-admissibility

- Initialize-Update-Read protocol, for concurrent accesses
- Want to conservatively extend Esterel's "Write-Read protocol" (must do emit *before* testing)
- But does Esterel *always* follow write-read protocol?

Write After Read Revisited

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module WriteAfterRead
output x, y, z;

emit x;
[
  present x then
    emit y
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||
  present y then
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end
```

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SCL version

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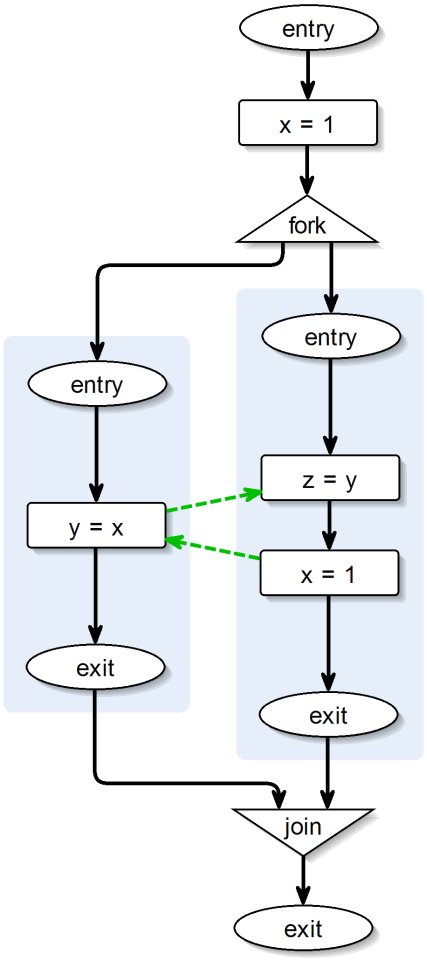

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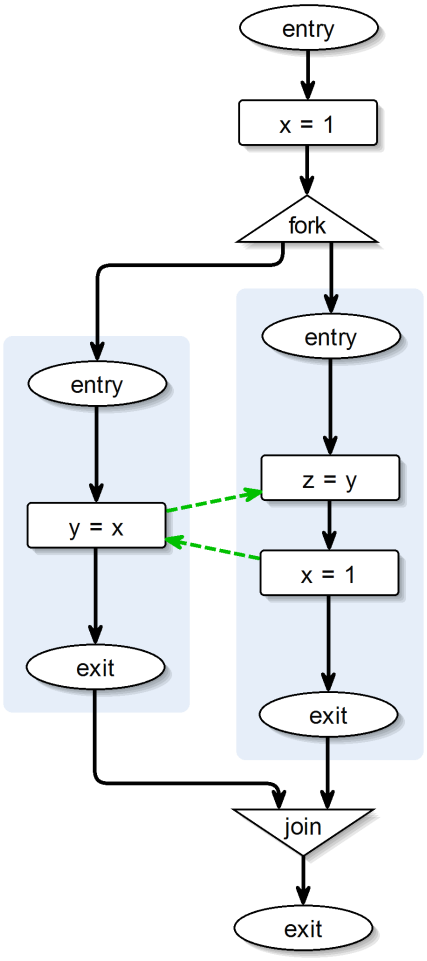

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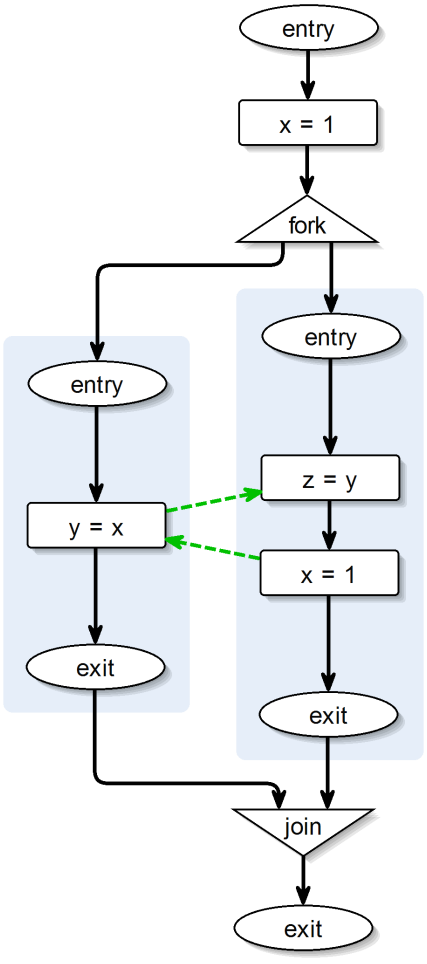

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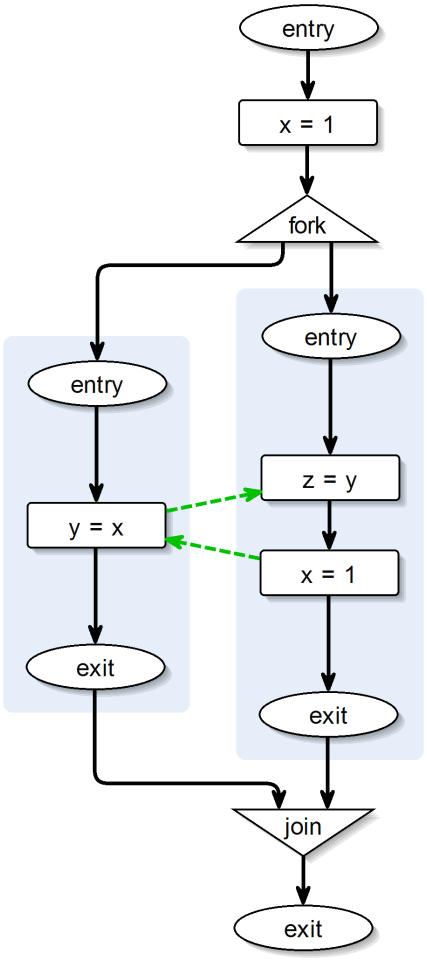

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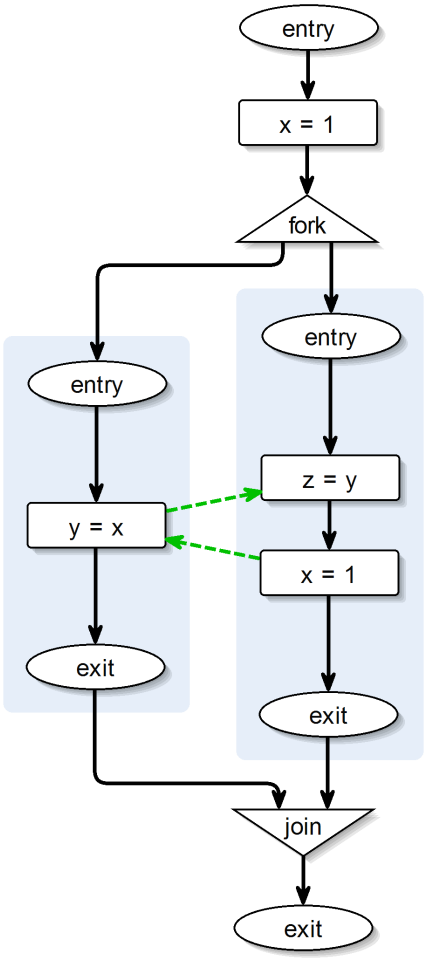

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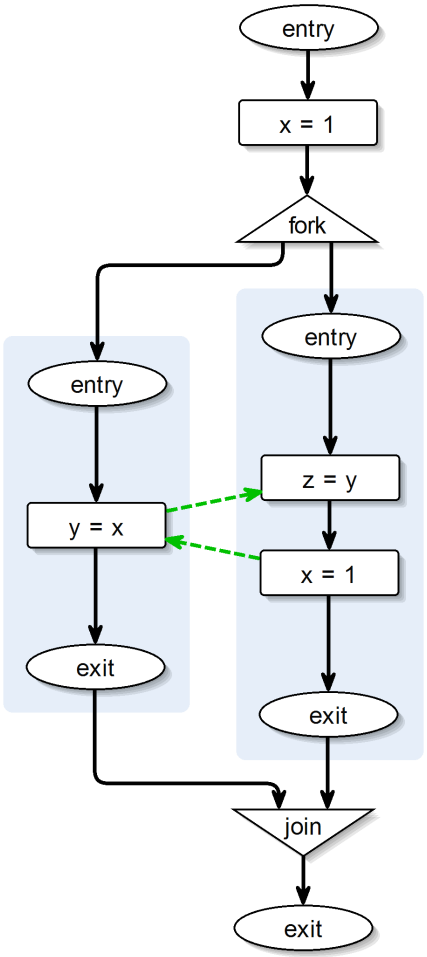

- Concurrent emit *after* present test
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- One approach: permit concurrent ineffective writes after read

Ineffectiveness – 1st Try [TR, Sec. 5.2]

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- Consider writes "ineffective" only if they do not change read!

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- $\rightarrow$ Replace "ineffectiveness" by "confluence"

Overview

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- Examples: *, $+$, $-$, max, and, or

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- E.g., `x = 0`, `x = 2*y+5`

Relative and Absolute Writes [Def. 4.2]

Relative writes, of type f ("increment" / "modify"): $x = f(x, e)$

- f must be a combination function
- Evaluation of e must be free of side effects
- Thus, schedules
  '$x = f(x, e_1); x = f(x, e_2)$' and
  '$x = f(x, e_2); x = f(x, e_1)$' yield same result for x
- Thus, writes are confluent
- E.g., `x++`, `x = 5*x`, `x = x-10`

Absolute writes ("write" / "initialize"): $x = e$

- Writes that are not relative
- E.g., `x = 0`, `x = 2*y+5`, `x = f(z)`

iur Relations [Def. 4.3]

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- $n_1 \rightarrow_{ww} n_2$ iff n_1 and n_2 both initialize x or both perform updates of different type. We call this a ww conflict
- $n_1 \rightarrow_{iu} n_2$ iff n_1 initializes x and n_2 updates x
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Since $n_1 \rightarrow_{ww} n_2$ implies $n_2 \rightarrow_{ww} n_1$:

- abbreviate the conjunction of $n_1 \rightarrow_{ww} n_2$ and $n_2 \rightarrow_{ww} n_1$ with $n_1 \leftrightarrow_{ww} n_2$

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- abbreviate the conjunction of $n_1 \rightarrow_{ww} n_2$ and $n_2 \rightarrow_{ww} n_1$ with $n_1 \leftrightarrow_{ww} n_2$
- by symmetry $\rightarrow_{ww}$ implies $\leftrightarrow_{ww}$

Confluence of Nodes [Def. 4.4]

Given:

- Valid configuration (C, M) of SCG
- Nodes $n_1, n_2 \in N$

n_1, n_2 are conflicting in (C, M) iff

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written: $n_1 \sim_{(C,M)} n_2$, iff

- $\nexists$ Sequence of micro steps $(C, M) \twoheadrightarrow_{\mu s} (C', M')$
  such that n_1 and n_2 are conflicting in (C', M')

Notes on Confluence

(From definition:) $n_1 \sim_{(C,M)} n_2$ iff

- $\nexists$ Sequence of micro steps $(C, M) \twoheadrightarrow_{\mu s} (C', M')$ such that n_1 and n_2 are conflicting in (C', M')

Observations I

- Confluence is taken *relative* to valid configurations (C, M) and *indirectly* as the absence of conflicts
- Instead of requiring that confluent nodes commute with each other for *arbitrary* memories, we only consider those configurations (C', M') that are *reachable* from (C, M)
- *E. g.*, if it happens for a given program that in all memories M' reachable from a configuration (C, M) two expressions ex_1 and ex_2 evaluate to the same value, then the assignments $x = ex_1$ and $x = ex_2$ are confluent in (C, M)

Notes on Confluence

(From definition:) $n_1 \sim_{(C,M)} n_2$ iff

- $\nexists$ Sequence of micro steps $(C, M) \twoheadrightarrow_{\mu s} (C', M')$ such that n_1 and n_2 are conflicting in (C', M')

Observations II

- Similarly, if the two assignments are never jointly active in any reachable continuation pool C', they are confluent in (C, M), too
- Thus, statements may be confluent for some program relative to some reachable configuration, but not for other configurations or in another program

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Observations II

- Similarly, if the two assignments are never jointly active in any reachable continuation pool C', they are confluent in (C, M), too
- Thus, statements may be confluent for some program relative to some reachable configuration, but not for other configurations or in another program
- However, notice that relative writes of the same type are confluent in the absolute sense, *i. e.*, for all valid configurations (C, M) of all programs

Notes on Confluence

(From definition:) $n_1 \sim_{(C,M)} n_2$ iff

- $\nexists$ Sequence of micro steps $(C, M) \twoheadrightarrow_{\mu s} (C', M')$ such that n_1 and n_2 are conflicting in (C', M')

Observations III

- Confluence $n_1 \sim_{(C,M)} n_2$ requires conflict-freeness for *all* configurations (C', M') reachable from (C, M) by *arbitrary* micro-sequences under *free scheduling*
- Will use this notion of confluence to define the restricted set of *SC-admissible* macro ticks

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- Will use this notion of confluence to define the restricted set of *SC-admissible* macro ticks
- Since compiler will ensure SC-admissibility of the execution schedule,
  one might be tempted to define confluence relative to these SC-admissible schedules;
  however, this would result in a logical cycle

Notes on Confluence

(From definition:) $n_1 \sim_{(C,M)} n_2$ iff

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- This relative view of confluence keeps the scheduling constraints on SC-admissible macro ticks sufficiently weak

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- However, more nodes may become confluent in later configurations, because some conflicting configurations are no longer reachable
- Exploit this in following definition of confluence *of node instances* by making confluence of node instances within a macro tick relative to the index position at which they occur

Confluence of Node Instances [Def. 4.5]

Given:

- Macro tick R
- (C_i, M_i) for $0 \leq i \leq \mathit{len}(R)$, the configurations of R
- Node instances $ni_1 = (n_1, i_1)$ and $ni_2 = (n_2, i_2)$ in R

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Call node instances confluent in R, written $ni_1 \sim_R ni_2$, iff

- for $i = min(i_1, i_2) - 1$
- $n_1 \sim_{(C_i, M_i)} n_2$

InEffective2 Revisited

```
1  module InEffective2
2  output bool x = false;
3    int y;
4  {
5   fork
6     if (!x) {
7       y = 1;
8       x = x xor true
9     }
10    else
11      y = 0
12   par
13    x = x xor true;
14   join
15 }
```

Recall sequence L6; L7; L8; L13:

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- Q: Is L13 ineffective *relative to L6*?

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- A: No!
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→ Def. of SC-admissibility – specifically, the underlying scheduling relations – uses confluence condition

Scheduling Relations [Def 4.6]

Given:

- Macro tick R with
- Node instances $ni_{1,2} = (n_{1,2}, i_{1,2})$, *i. e.*, $1 \leq i_{1,2} \leq len(R)$ and $n_{1,2} = R(i_{1,2})$
- $ni_{1,2}$ concurrent in R, *i. e.*, $ni_1 \mid_R ni_2$
- $ni_{1,2}$ not confluent in R, *i. e.*, $ni_1 \not\sim_R ni_2$

Then:

- $ni_1 \rightarrow^R_\alpha ni_2$ iff $n_1 \rightarrow_\alpha n_2$ for some $\alpha \in \alpha_{iur}$
- $ni_1 \rightarrow^R ni_2$ iff $i_1 < i_2$; *i. e.*, ni_1 happens before ni_2 in R.

Sequential Admissibility [Def. 4.7]

A macro tick R is SC-admissible iff

- for all node instances $ni_{1,2} = (n_{1,2}, i_{1,2})$ in R, with $1 \leq i_{1,2} \leq \mathit{len}(R)$ and $n_{1,2} = R(i_{1,2})$,
- for all $\alpha \in \alpha_{iur}$

the scheduling condition SC_α holds:

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- for all $\alpha \in \alpha_{iur}$

the scheduling condition SC_α holds:
if $ni_1 \rightarrow^R_\alpha ni_2$ then $ni_1 \rightarrow^R ni_2$.

A run for an SCG is SC-admissible if all macro ticks R in this run are SC-admissible.

SC-admissibility vs. Determinacy

SC-admissibility vs. Determinacy

```
1  module NonDet
2  output bool x = false, y = false;
3  {
4   fork { // Thread CheckX
5    if (!x)
6     y = true;
7   }
8   par { // Thread CheckY
9    if (!y)
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11  }
12  join
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- Admissible runs?

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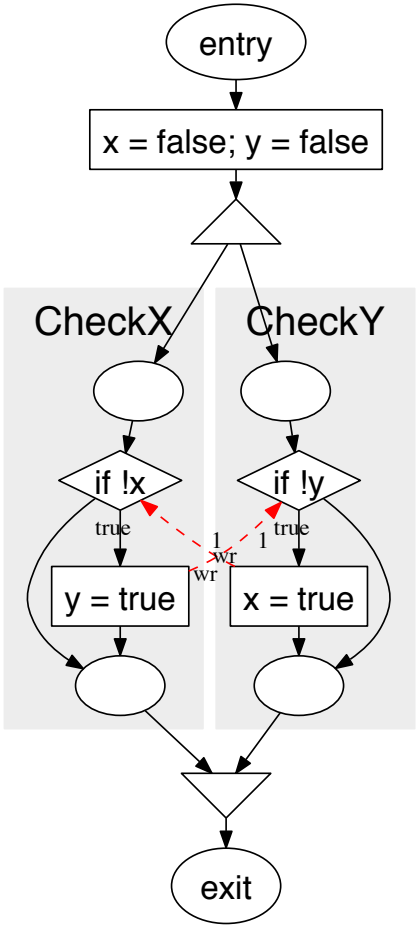

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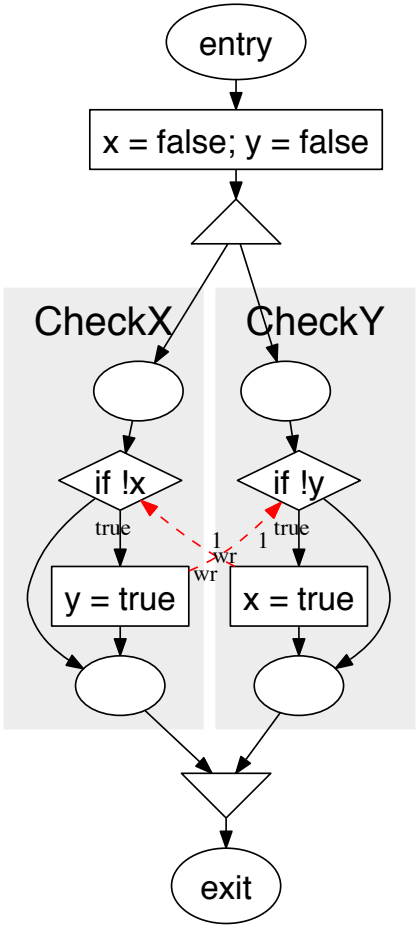

- Admissible runs? Yes, multiple
- Determinate? No

Thus: **SC-admissibility** $\not\Rightarrow$ **Determinacy**

SC-admissibility vs. Determinacy

SC-admissibility vs. Determinacy

```
1  module Fail
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SC-admissibility vs. Determinacy

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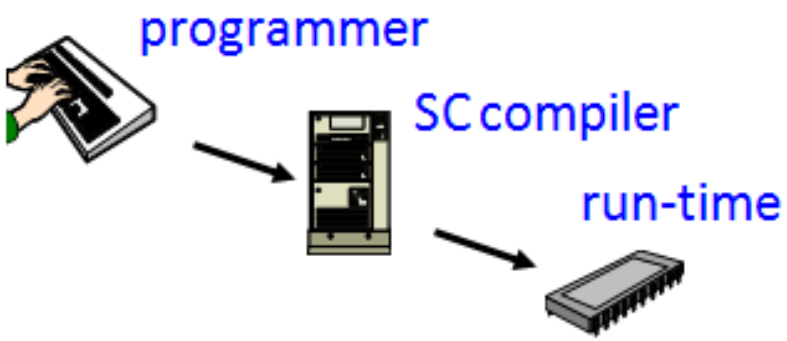
Thus: **Determinacy $\not\Rightarrow$ SC-admissibility**

Sequential Constructiveness [Def. 4.8]

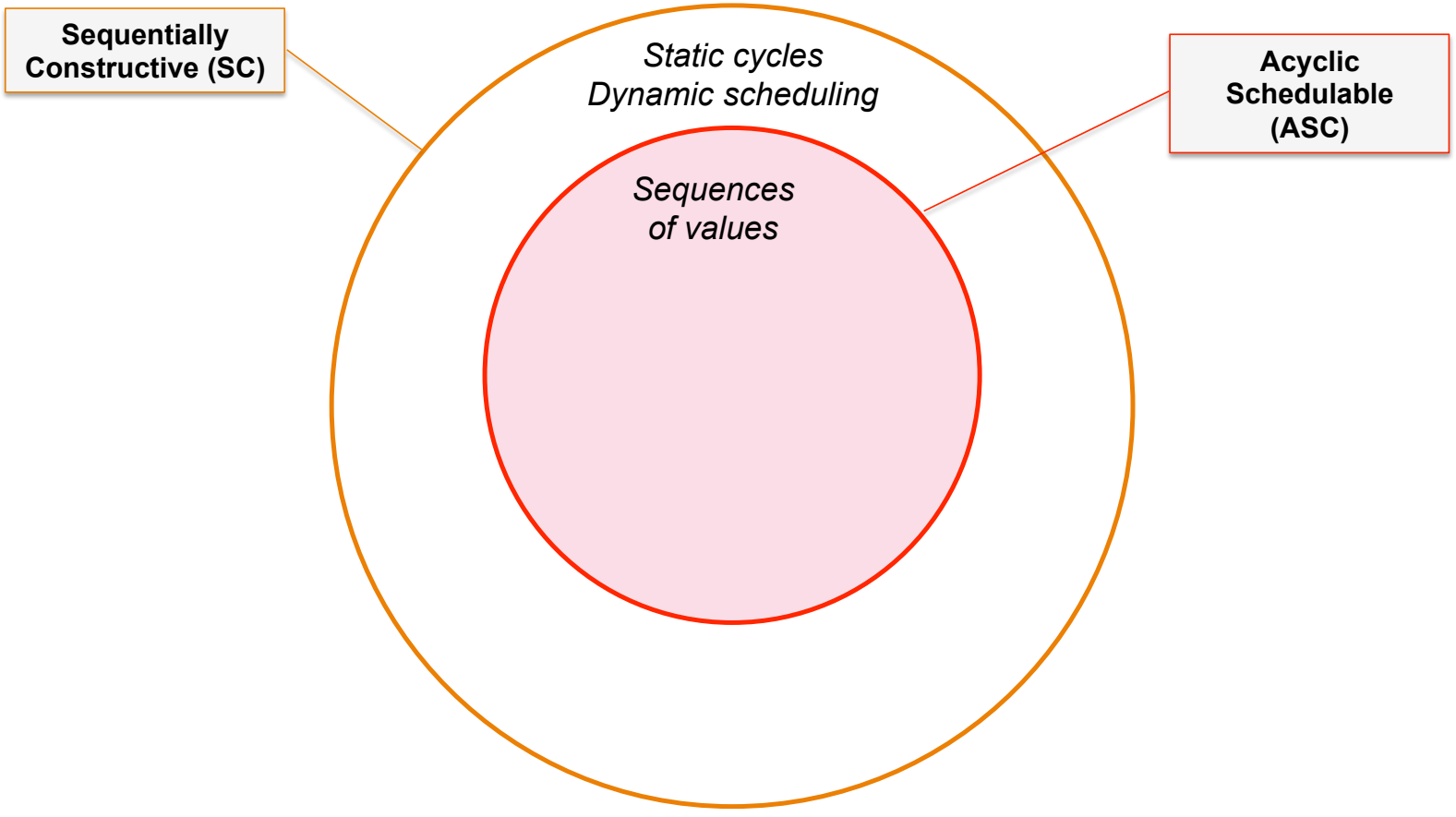


Definition: A program P is sequentially constructive (SC) iff for each initial configuration and input sequence:

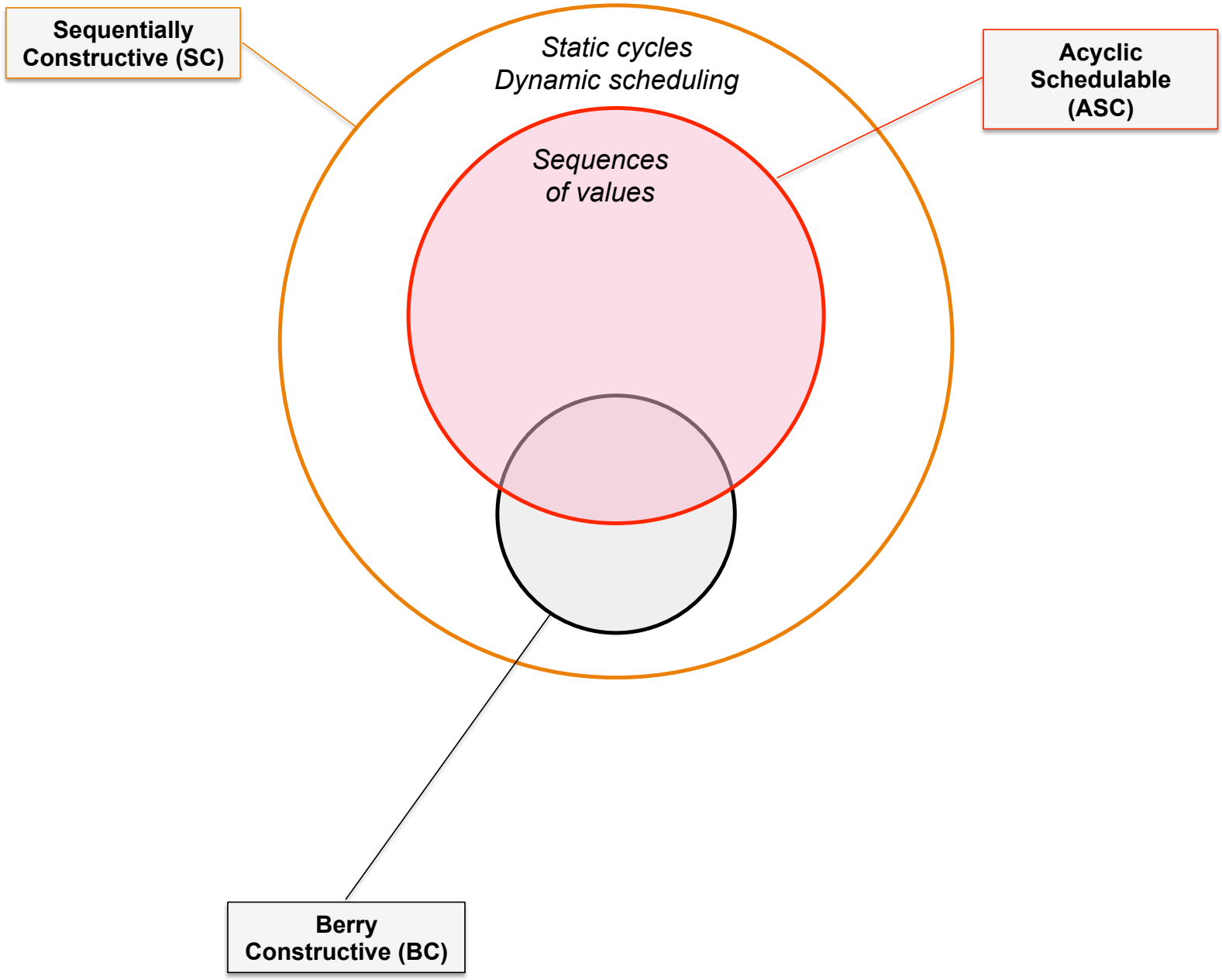
1. There exists an SC-admissible run (P is reactive)
2. Every SC-admissible run generates the same determinate sequence of macro responses (P is determinate)

Overview

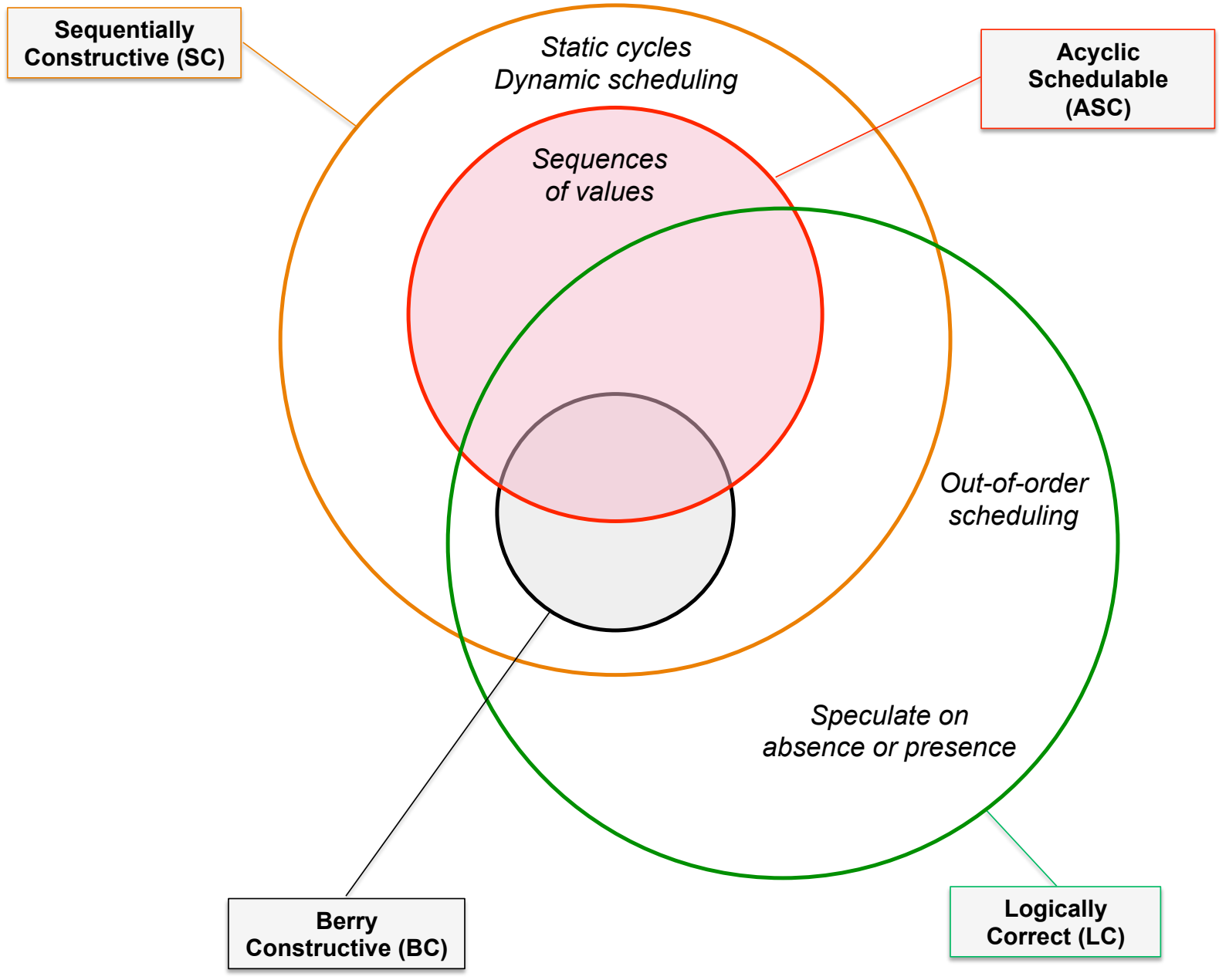
Synchronous Program Classes [TR, Sec. 9]



Synchronous Program Classes [TR, Sec. 9]



Synchronous Program Classes [TR, Sec. 9]



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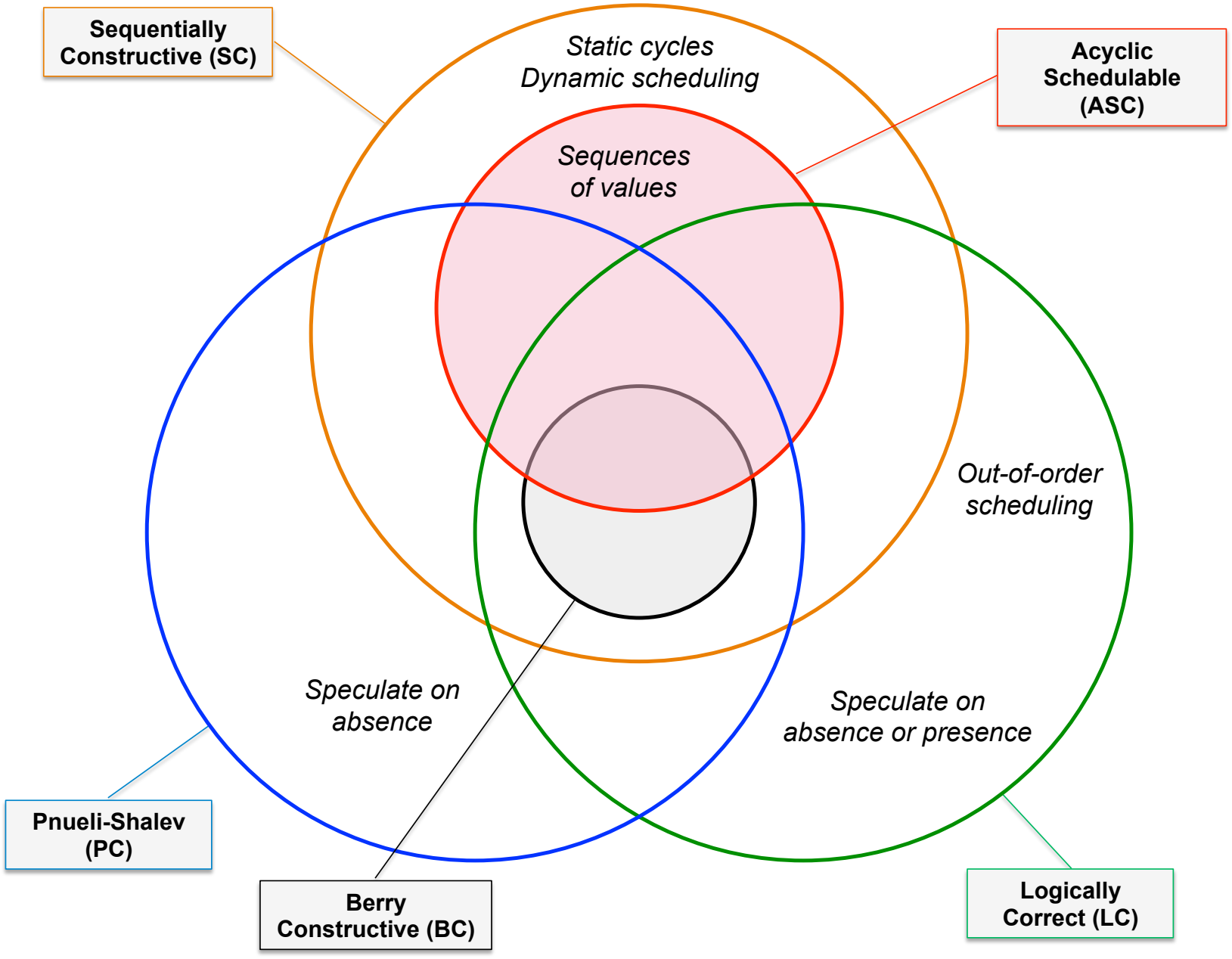
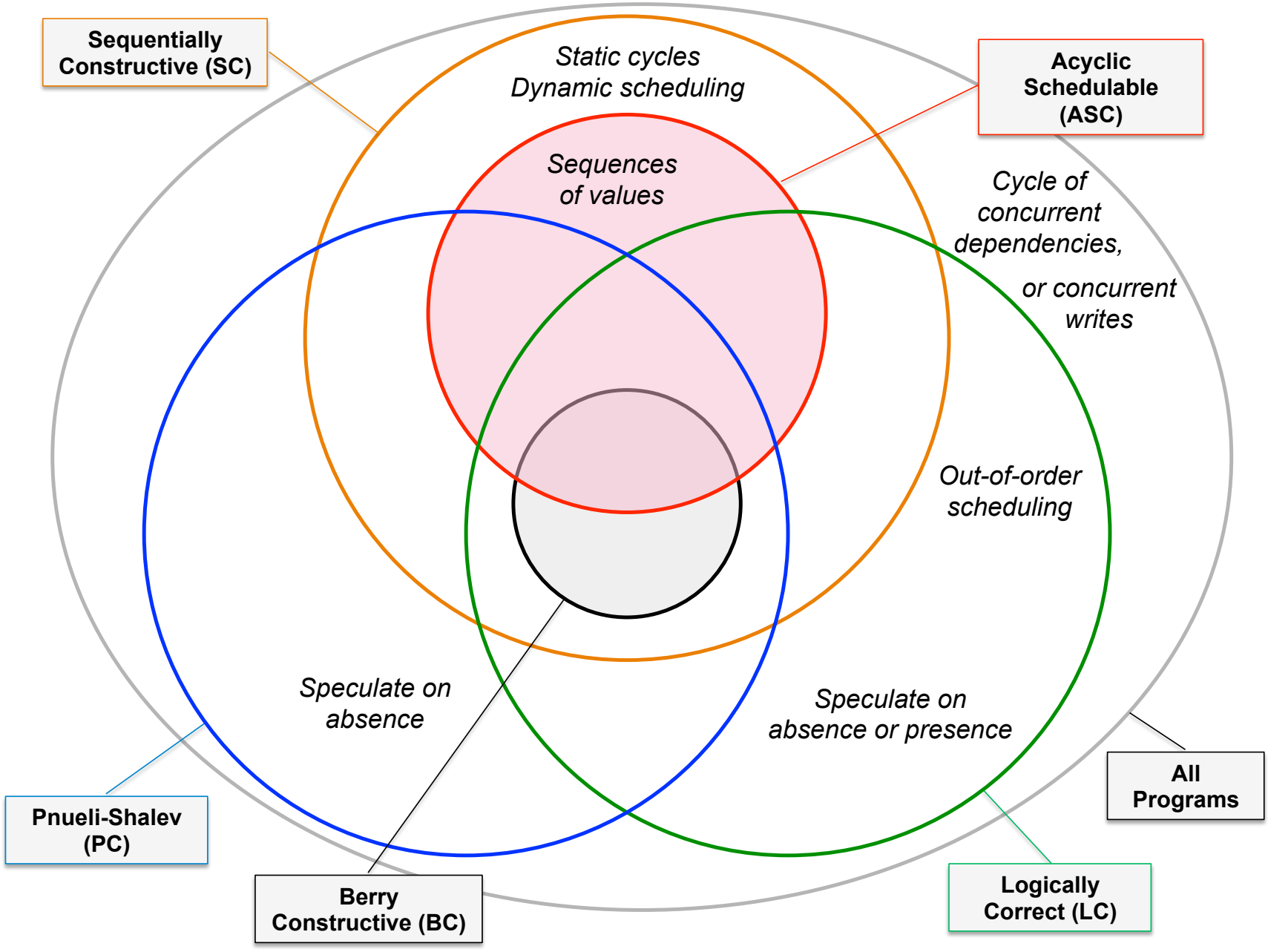
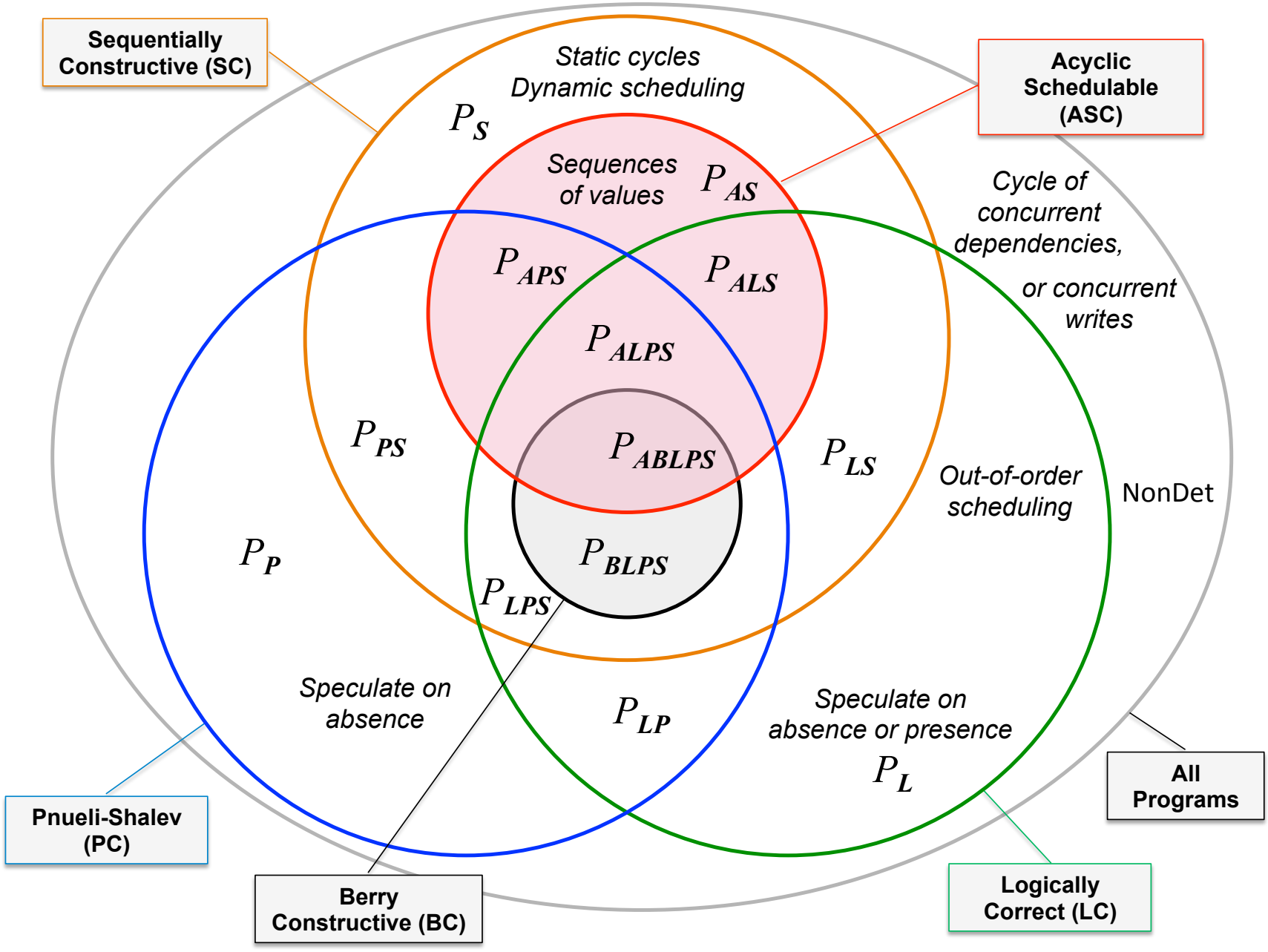


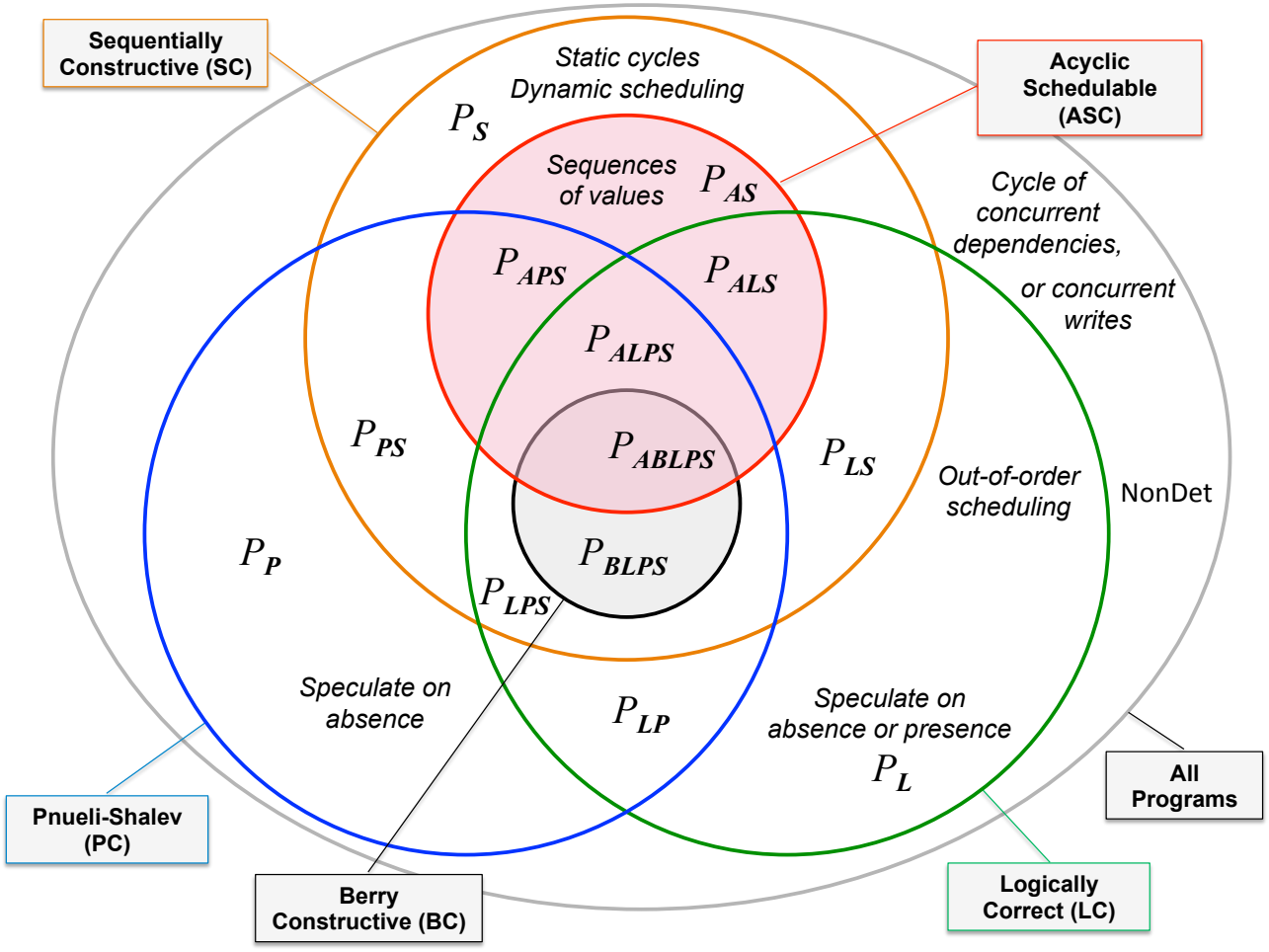
Synchronous Program Classes [TR, Sec. 9]



Synchronous Program Classes [TR, Sec. 9]

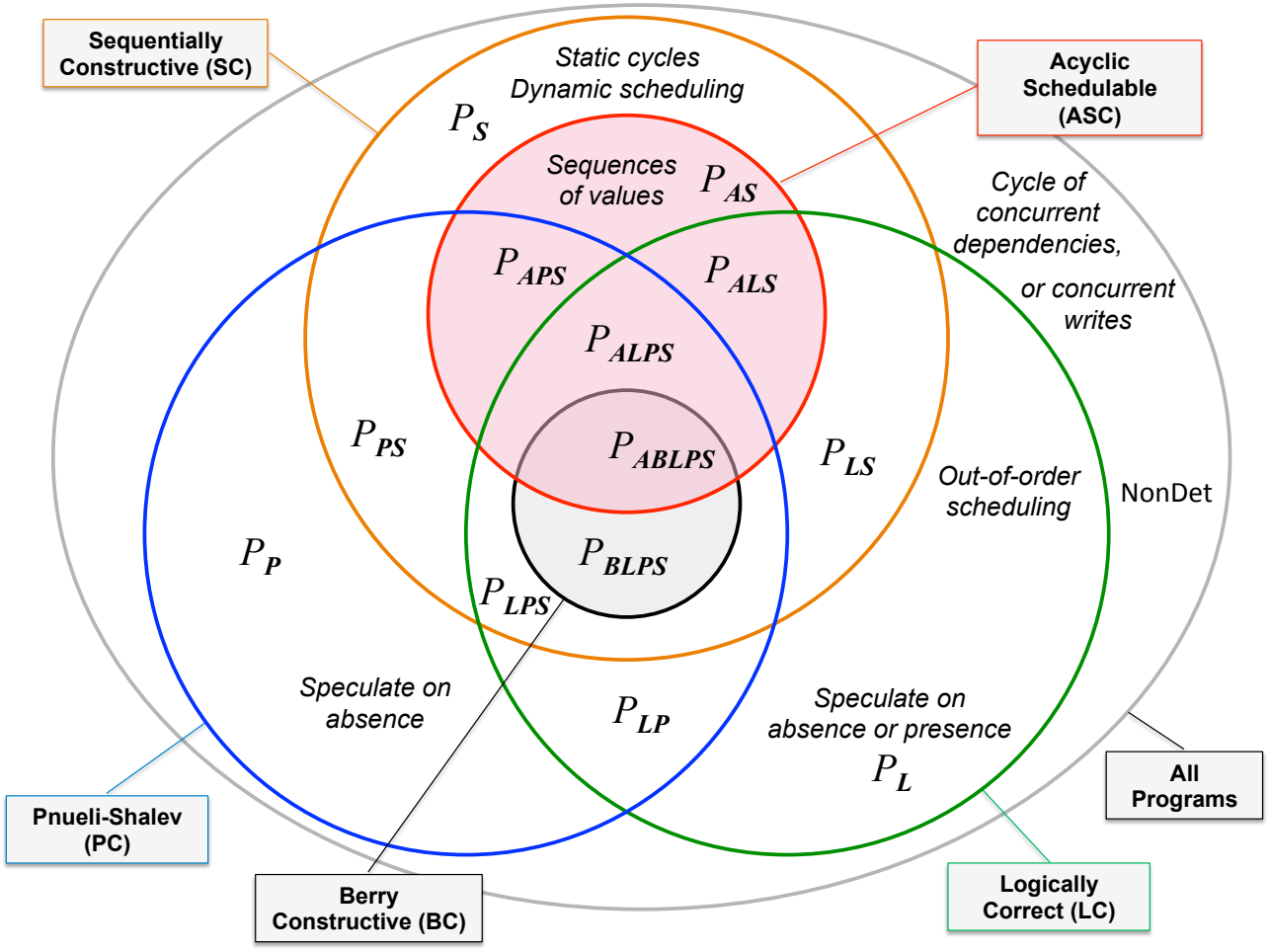


Synchronous Program Classes



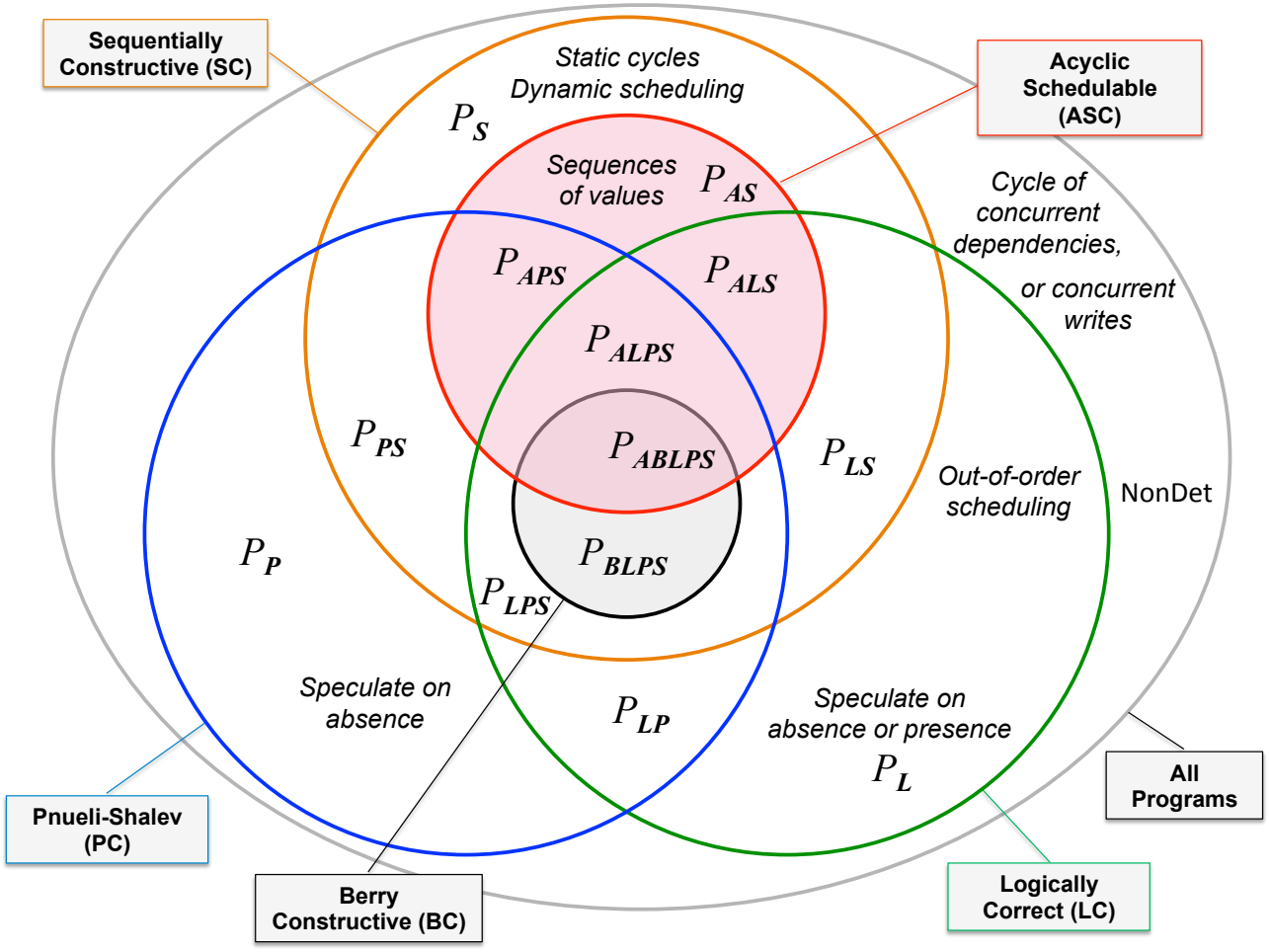
Example $P_{APS} =$

Synchronous Program Classes



Example P_{APS} = if (x) x = 1

Synchronous Program Classes



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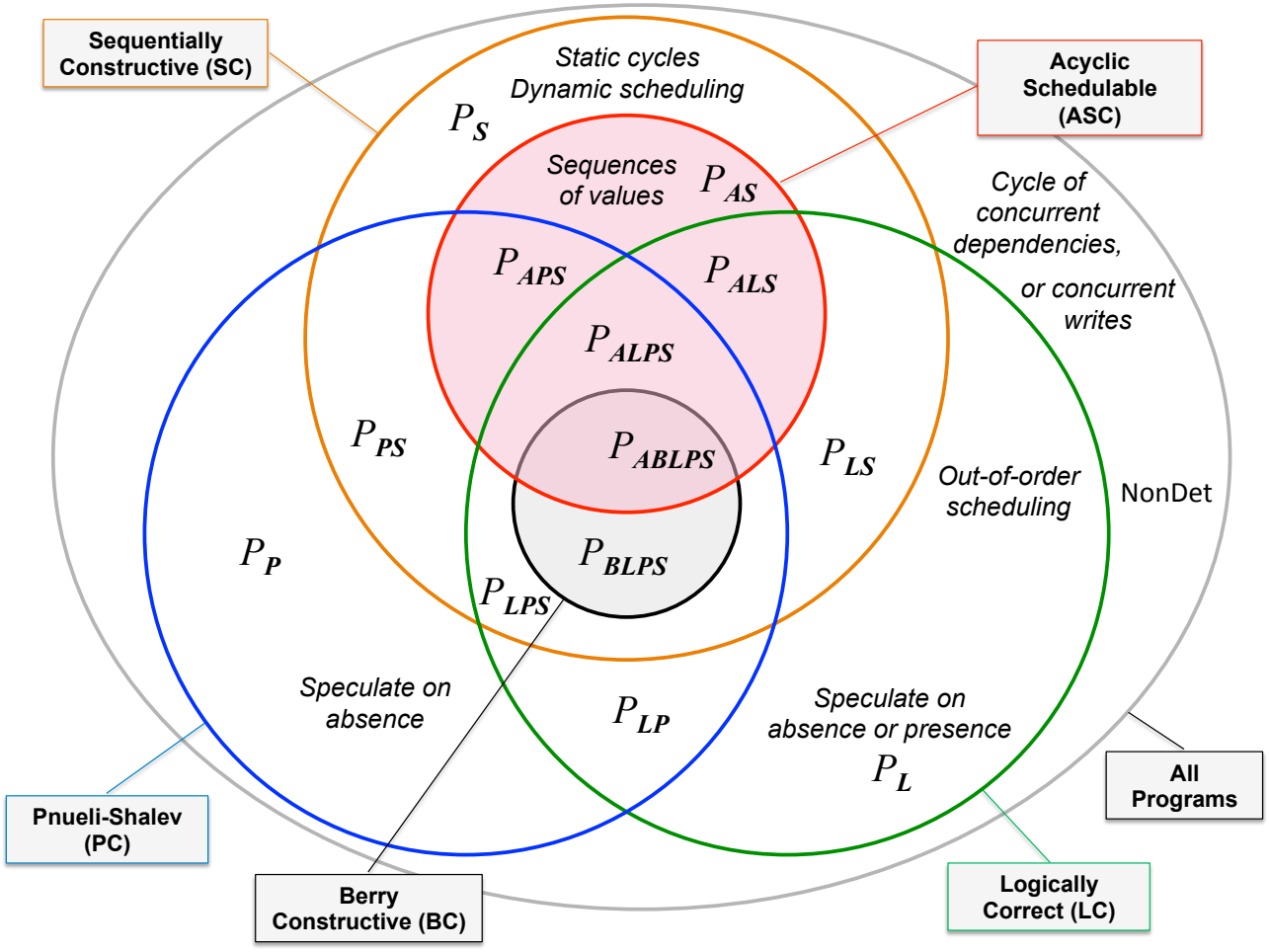
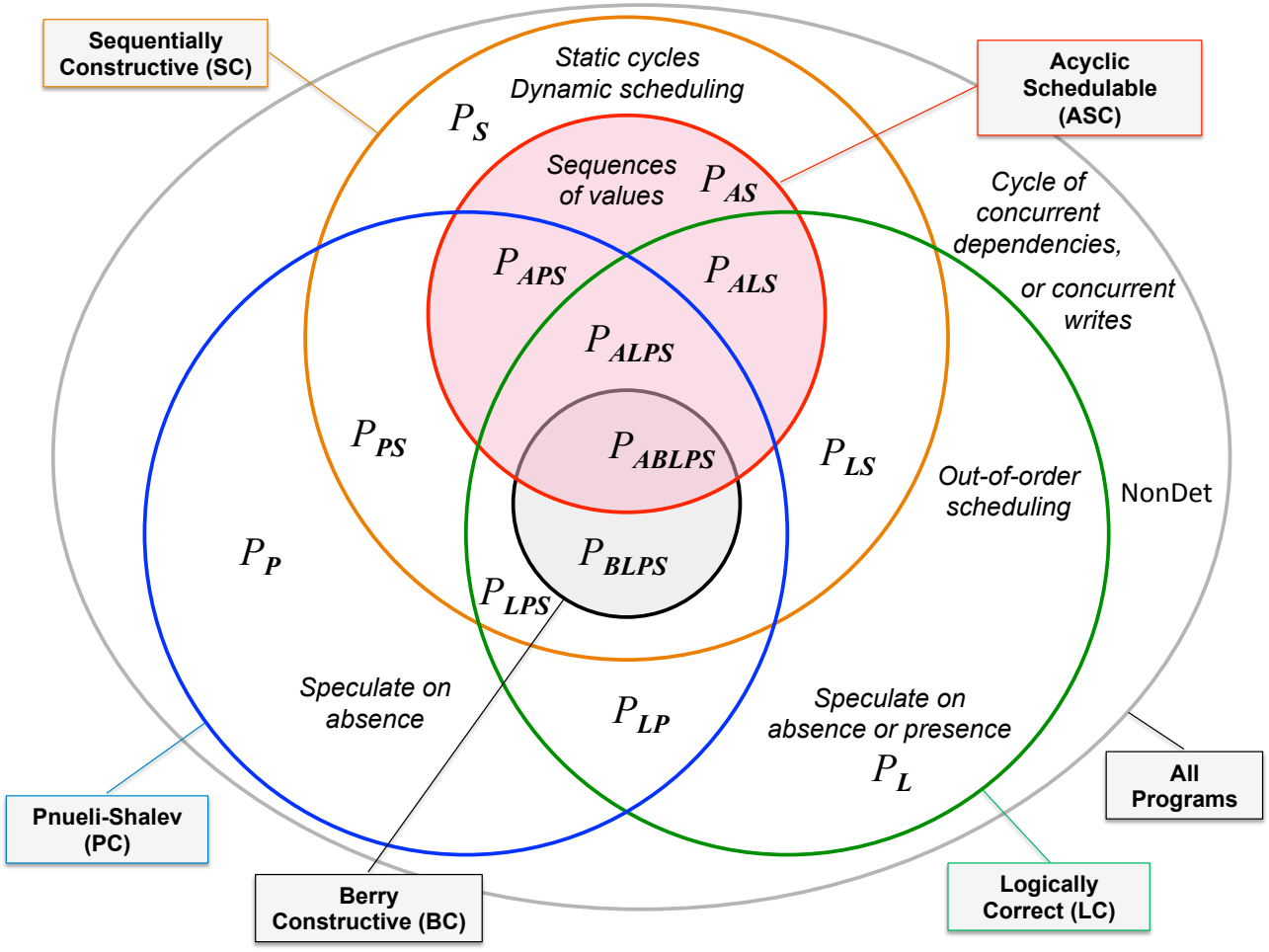
Synchronous Program Classes



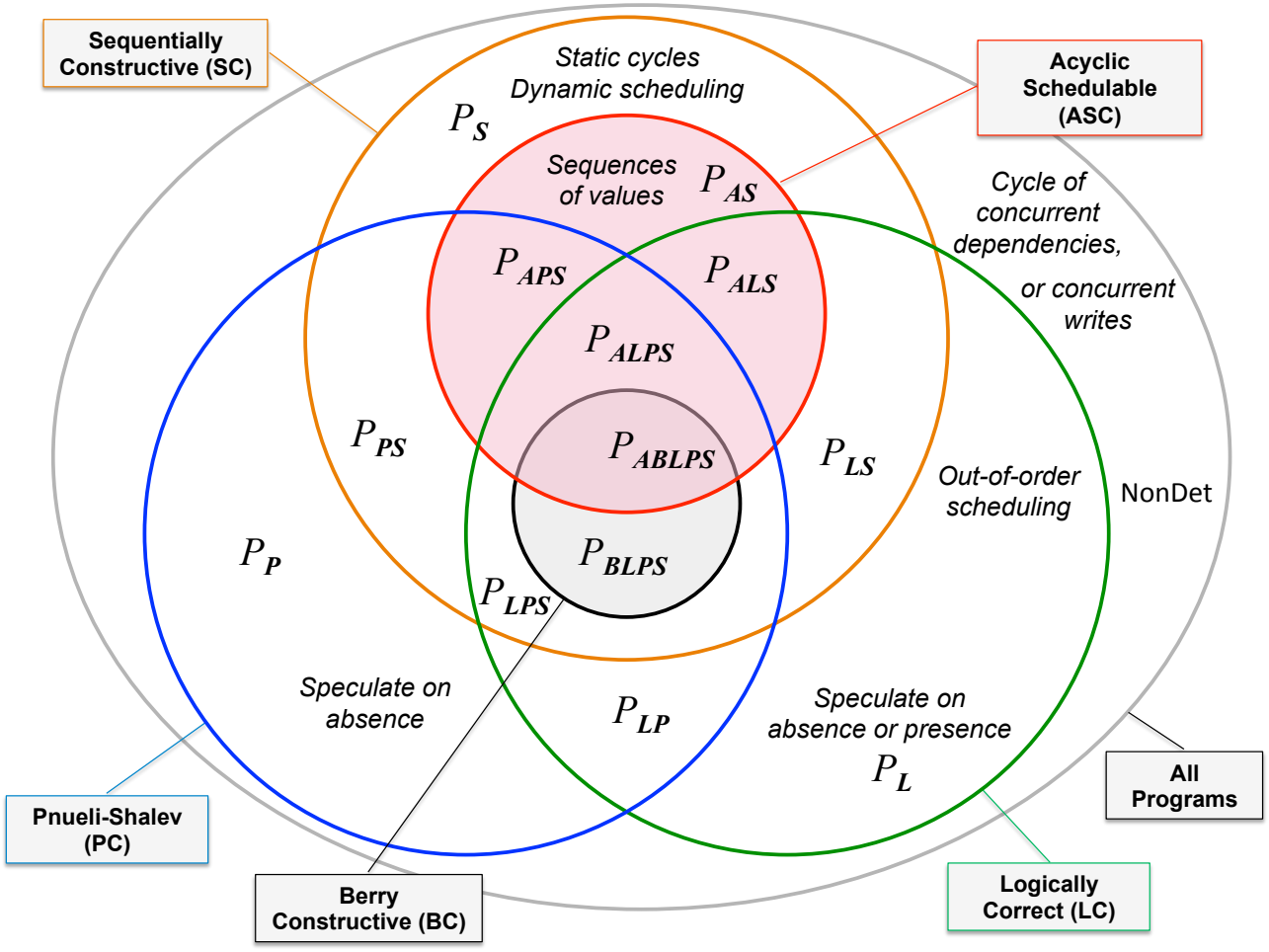
Example P_{AS} = if (!x) x = 1

Synchronous Program Classes



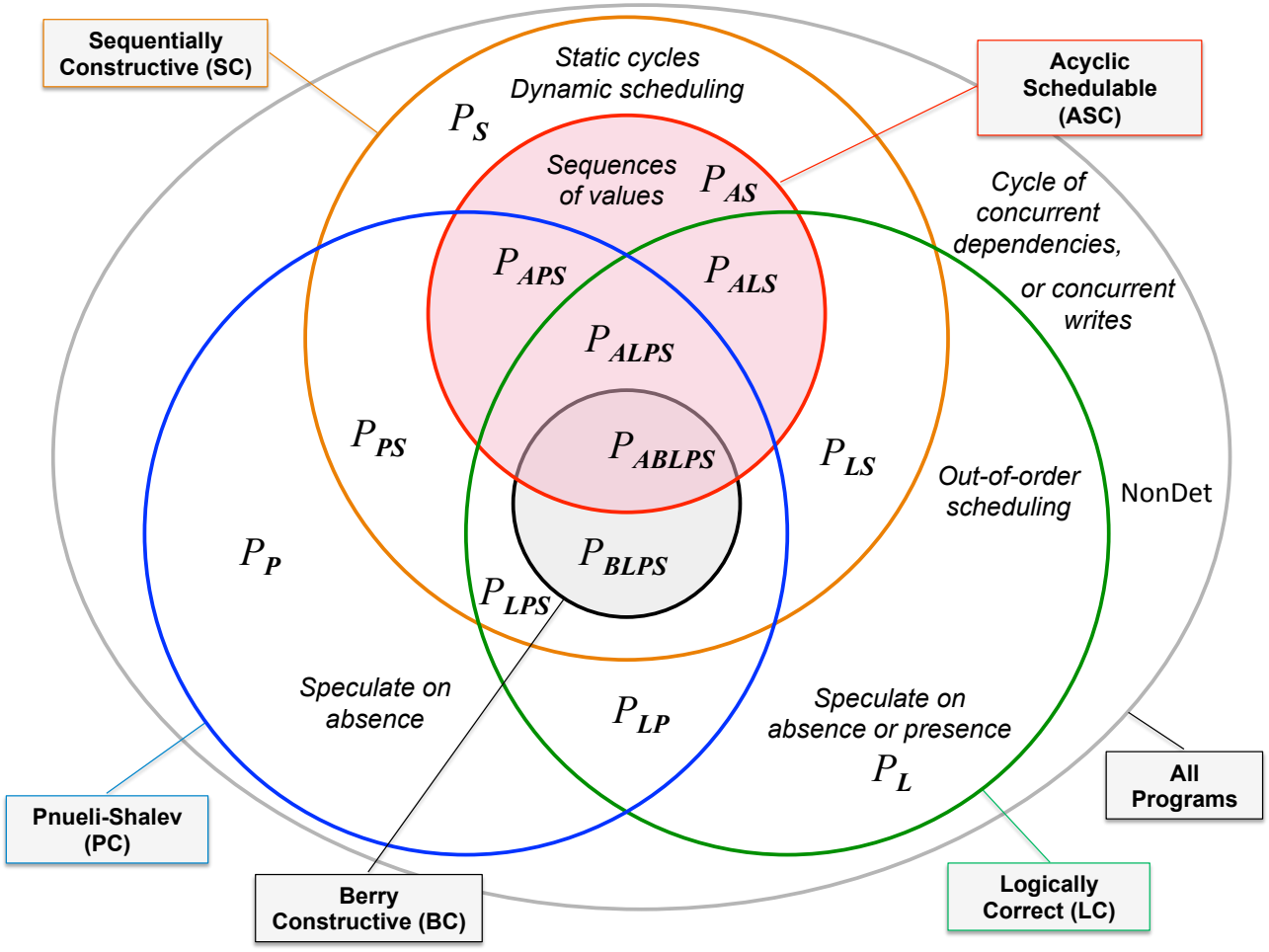
Example $P_{ALS} =$

Synchronous Program Classes



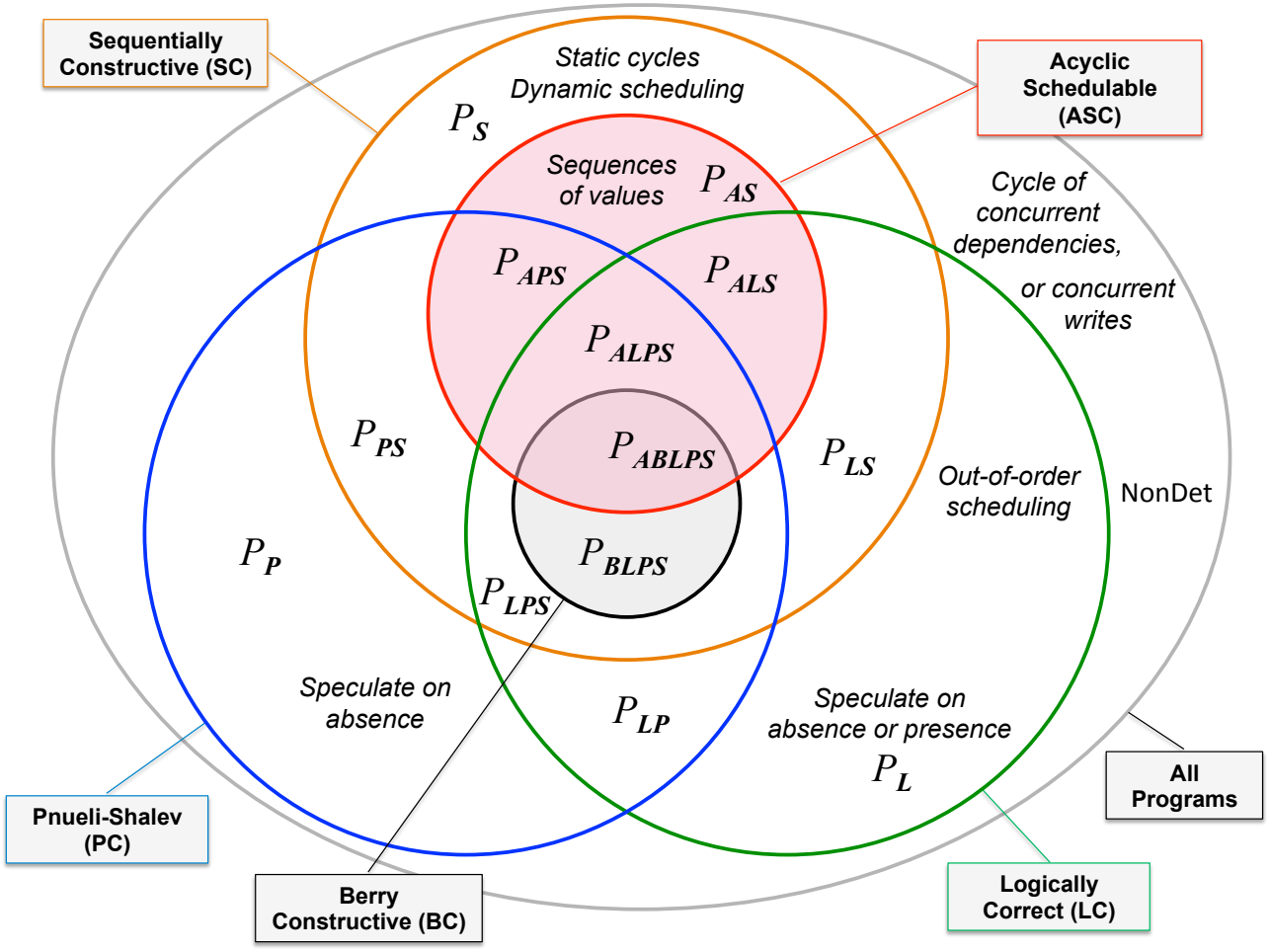
Example P_{ALS} = if (!x) x = 1 else x = 1

Synchronous Program Classes



Example $P_{ALPS} =$

Synchronous Program Classes



Example P_{ALPS} = if (!x && y) {x = 1; y = 1}

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Underlying idea of sequential constructiveness rather simple

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- Prescriptive instead of descriptive sequentiality
- Thus circumventing "spurious" causality problems
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- Thus circumventing "spurious" causality problems
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However, precise definition of SC MoC not trivial

- Challenging to ensure conservativeness relative to Berry-constructiveness
- Plain initialize-update-read protocol does not accomodate, *e. g.*, signal re-emissions
- Restricting attention to *concurrent*, *non-confluent* node instances is key

Conclusions

- Clocked, **synchronous model of execution** for **imperative, shared-memory multi-threading**
- Conservatively extends synchronous programming (Esterel) by **standard sequential control flow** (Java, C)
- $\Longrightarrow$ Deterministic concurrency with synchronous foundations, but without synchronous restrictions
  - ☺ Expressive and intuitive sequential paradigm
  - ☺ Predictable concurrent threads

Future Work

Plenty of extensions/adaptations possible . . .

- Alternative notions of sequential constructiveness:
  - A truly "constructive" approach that sharpens SC admissibility to determinate schedules
  - Extension of iur-protocol, *e. g.*, to model ForeC
- Improved synthesis & analysis — see also next lecture