Synchronous Languages—Lecture 07

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Esterel V—The Constructive Circuit Semantics

The 5-Minute Review Session

1. What is the derivative (*Ableitung*) of a program?

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4. Which semantics for Esterel exist?

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2. How is the *program transition* of an Esterel program defined?
3. How do program transitions express logical coherence?
4. Which semantics for Esterel exist?
5. What are the *constructive coherence laws*, how do they differ from the logical coherence law?

Overview

Translating Esterel to Circuits

- Can consider Esterel programs as SW or HW descriptions
- As it turns out, the HW-equivalent of constructiveness is that the synthesized circuit is delay-independent
  - This gives a firm, physical base for the constructive semantics we just considered

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- Can consider Esterel programs as SW or HW descriptions
- As it turns out, the HW-equivalent of constructiveness is that the synthesized circuit is delay-independent
  - This gives a firm, physical base for the constructive semantics we just considered
- Can in turn simulate this synthesized HW-circuit in SW
  - This is just what the Esterel v5 compiler does
  - Can then also take advantage of HW optimization techniques
  - Use BDD-based techniques to check constructiveness

Circuit Semantics—Introduction

```
module P1:
input I;
output O;
signal S1, S2 in
  present I then emit S1 end
||
  present S1 else emit S2 end
||
  present S2 then emit O end
end signal
end module
```

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- Resulting circuit is acyclic
- Hence always stabilizes
- Reactive and deterministic

Circuit Semantics—Introduction

```
module P3:
output O;
present O else emit O end
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```

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Circuit Semantics—Introduction

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module P3:
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Circuit Semantics—Introduction

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module P3:
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circuit C3:
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- Resulting circuit never stabilizes
- Not reactive

Circuit Semantics—Introduction

```
module P4:
output O;
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end module
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Circuit Semantics—Introduction

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module P4:
output O;
present O then emit O end
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circuit C4:
$O = O$

Circuit Semantics—Introduction

```
module P4:
output O;
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end module
```

$\equiv$

circuit C4:
$O = O$

- Resulting circuit can stabilize at different values
- Not deterministic

Circuit Semantics—Introduction

```
module P9:
[
  present O1 then emit O1 end
||
  present O1 then
    present O2 else emit O2 end
  end
]
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circuit C9:

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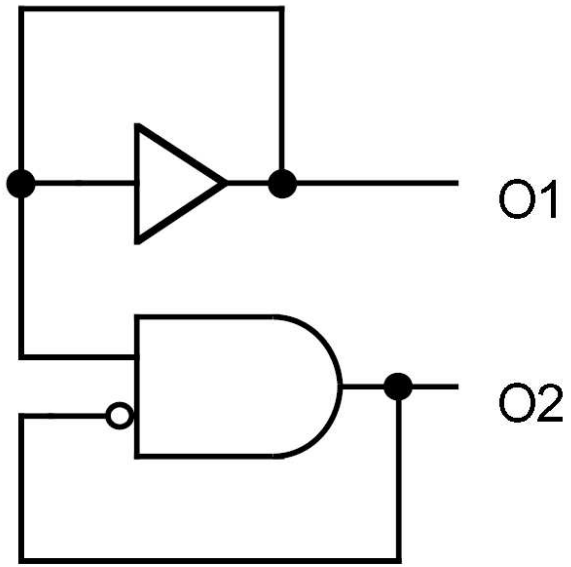

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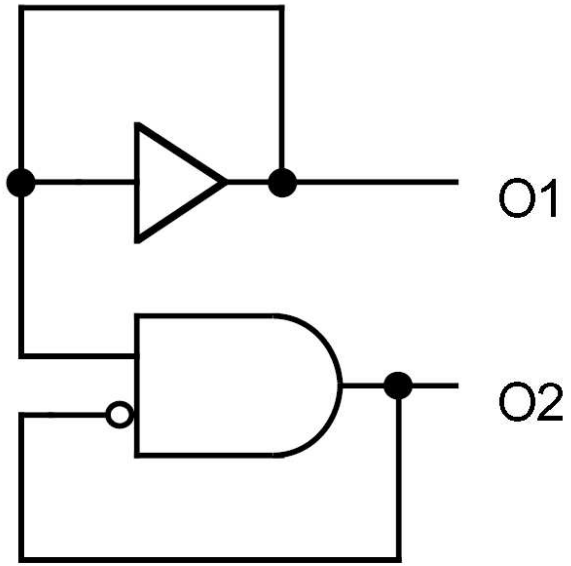

- Reactive and deterministic

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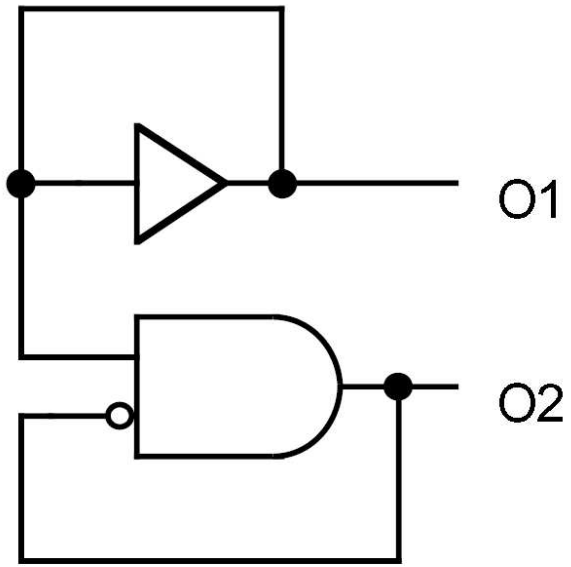

- Reactive and deterministic
- But not constructive!

Circuit Semantics—Introduction

```
module P12:
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≡

circuit C12:
$O = O \vee \neg O$

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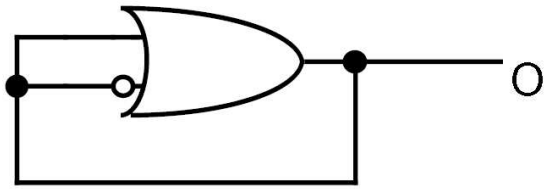

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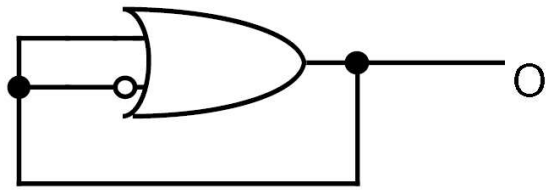

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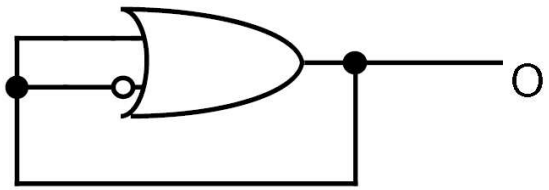

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- Meaning: If it stabilizes, there is only one possible value for each wire's voltage

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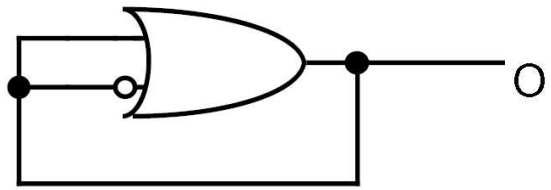

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- Meaning: If it stabilizes, there is only one possible value for each wire's voltage
- But: Does it always stabilize?

Circuit Semantics—Introduction

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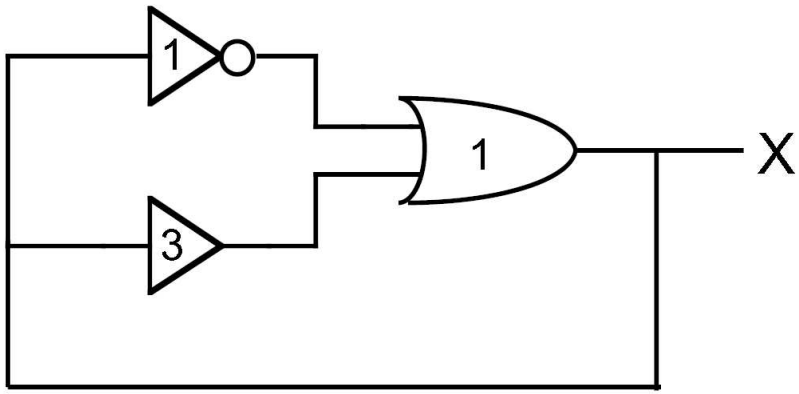

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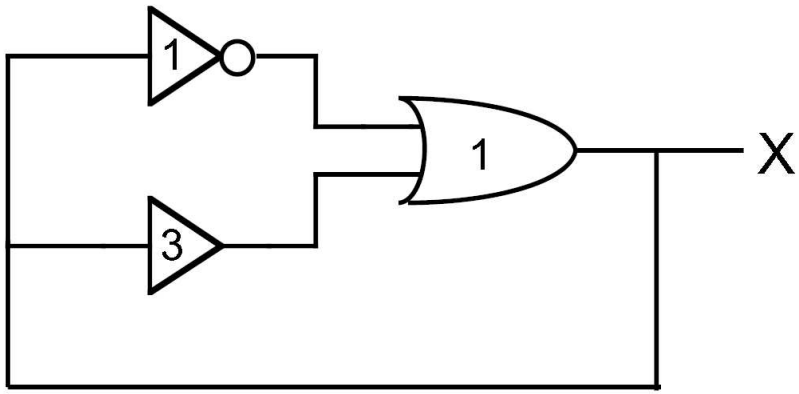

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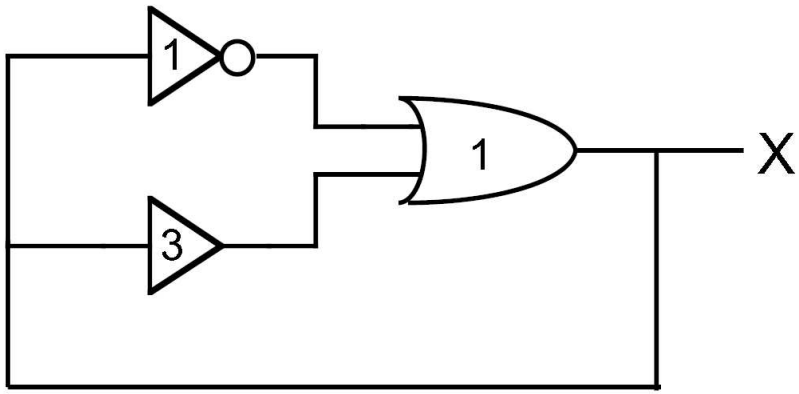

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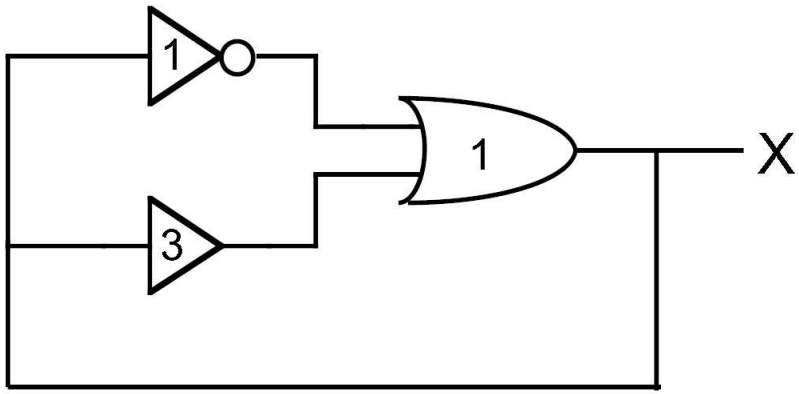

- Circuit is reactive and deterministic (Newtonian model)
- But: Circuit never stabilizes (Vibration model)
- **Hence: Electrical stabilization is not the conjunction of reactivity and determinism!**

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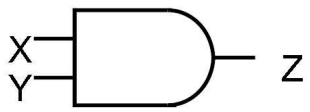
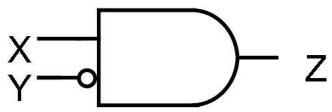
- Hence: Electrical stabilization does not require acyclicity
- In fact: Electrical stabilization equivalent to constructiveness

Constructive Circuits

Basic building blocks



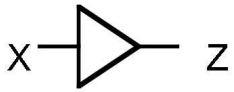
Z = X and Y



Z = X and not Y

Z = X or Y

Z = not (X or Y)



Z = X

Z = reg(X)

- Allow insertion of arbitrary delays
- Registers:
  - $reg(X) = 0 \rightarrow pre(X)$

Constructive Circuits

Constructive Boolean (intuitionistic) logic:

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- There is no law of excluded middle (x or not x $\rightarrow$ 1)!

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  - Propagation of 1's corresponds to *Must*-analysis
  - Propagation of 0s corresponds to *Cannot*-analysis

The Basic Circuit Translation

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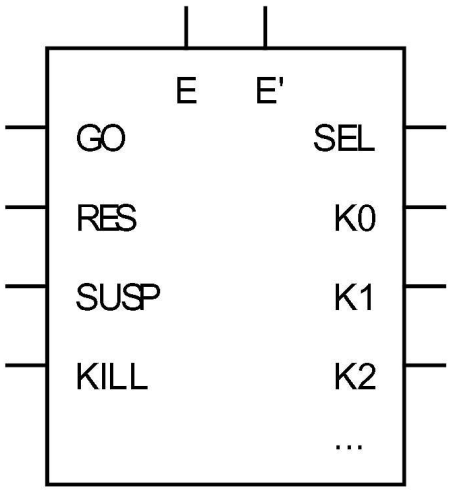
  - Associate registers with "1" statements (`pause`)
  - Associate combinational logic with all other statements
  - Build up program-circuit from subcircuits
  - Additional boot register to implement initial state
- Basic circuit translation does not address schizophrenia (see later)

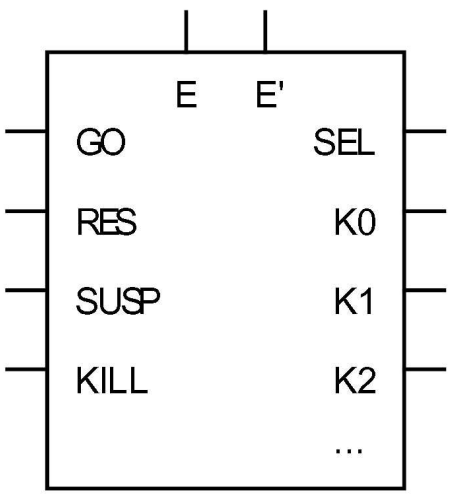
Interface for subcircuits



Inputs:

- GO: Starts statement afresh
- RES: Resumes execution of a selected statement
- SUSP: Suspend execution of the statement
  - Registers keep their current value unless killed because of the KILL input
- KILL: Unsets statement's registers in case of a trap exit

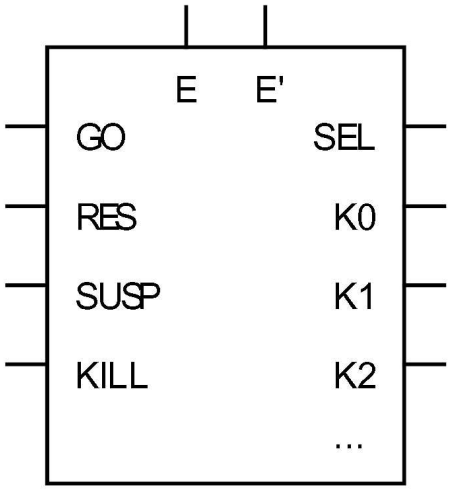
Interface for subcircuits contd.



Outputs:

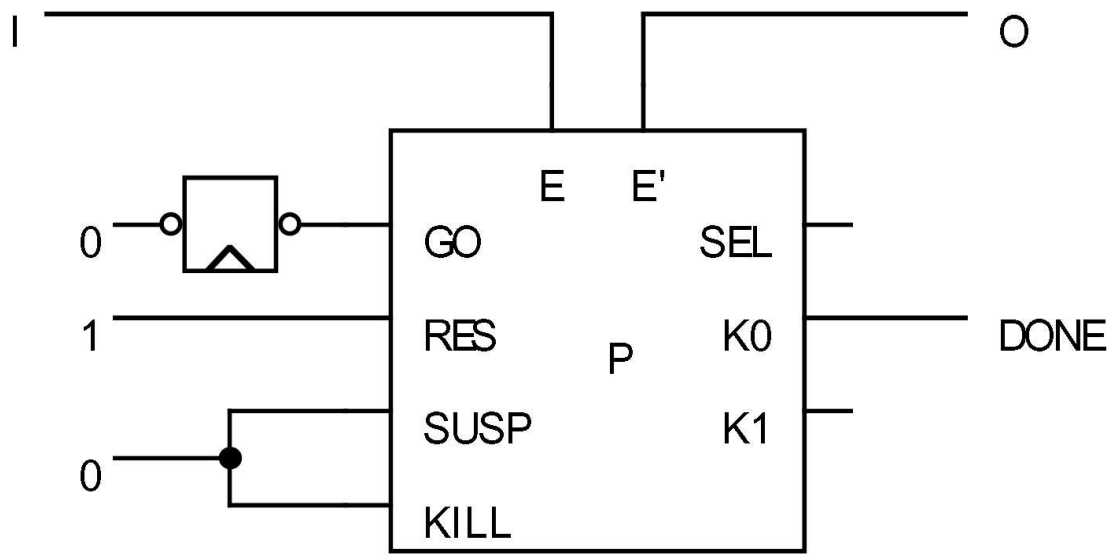
- SEL: Indicates that a state in statement is currently selected for resumption, i.e. that some internal pause register is set
  - Is simply the disjunction of the internal registers.
- K0, K1, ...: Completion codes (1-hot encoding)

Interface for subcircuits contd.



- E and E': input/output signal interface
- Are compound pins or buses
  - Contain one elementary pin per signal visible in the scope of the current statement.
- May freely extract specific signals s or s' out of E or E'.
- As for the K pins, the E' pins are explicitly unset when the statement is not executed
  - I.e. when $\neg($ GO $\vee$ (RES $\wedge$ SEL))

The Global Environment



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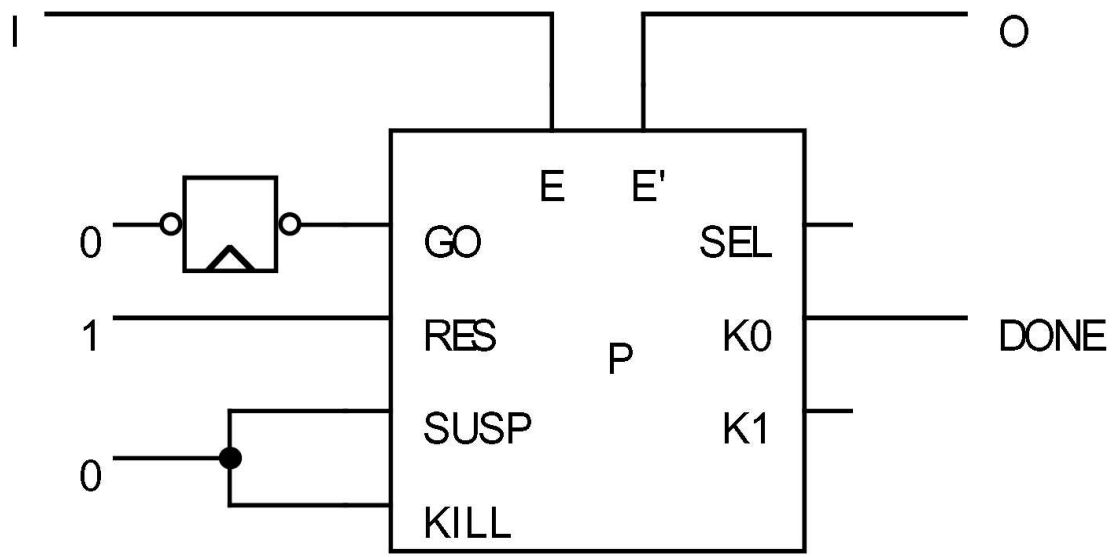
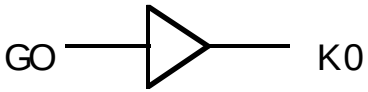


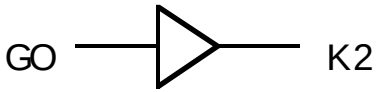
- Boot register sets GO input in initial instant
- At each clock cycle
  - set RES
  - clock the registers

Translating the Esterel Kernel

- Completion, with $k \neq 1$:



code 0



code 2

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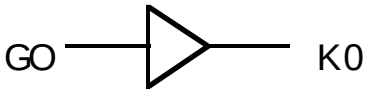

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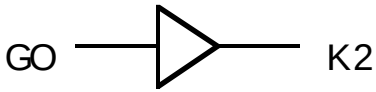

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- $k = 1$ (pause):

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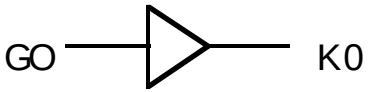

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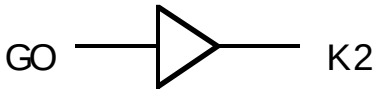
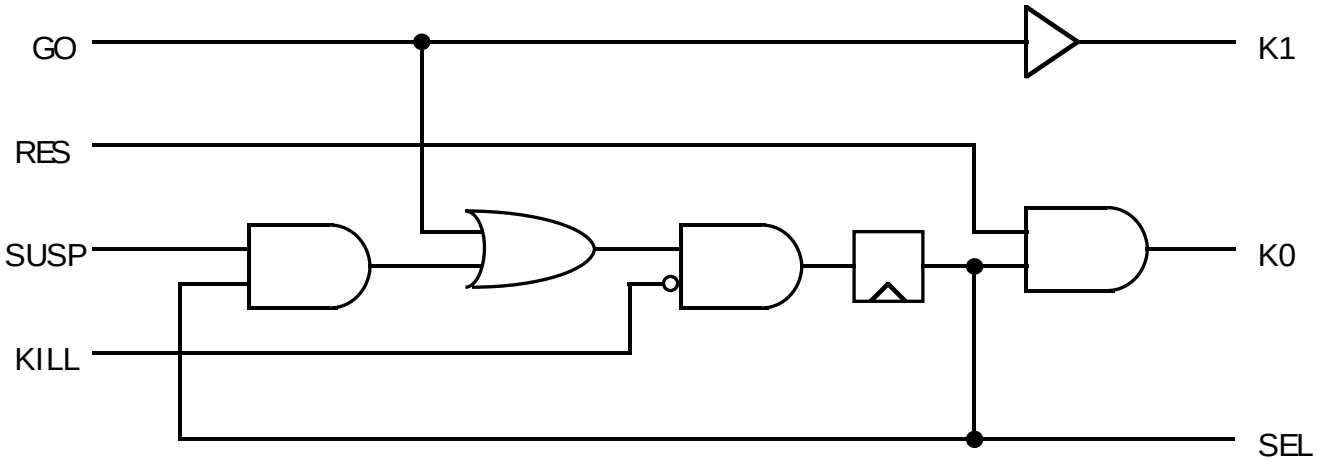


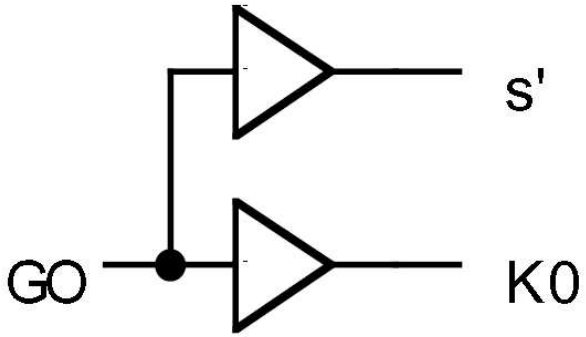
code 2

- $k = 1$ (pause):



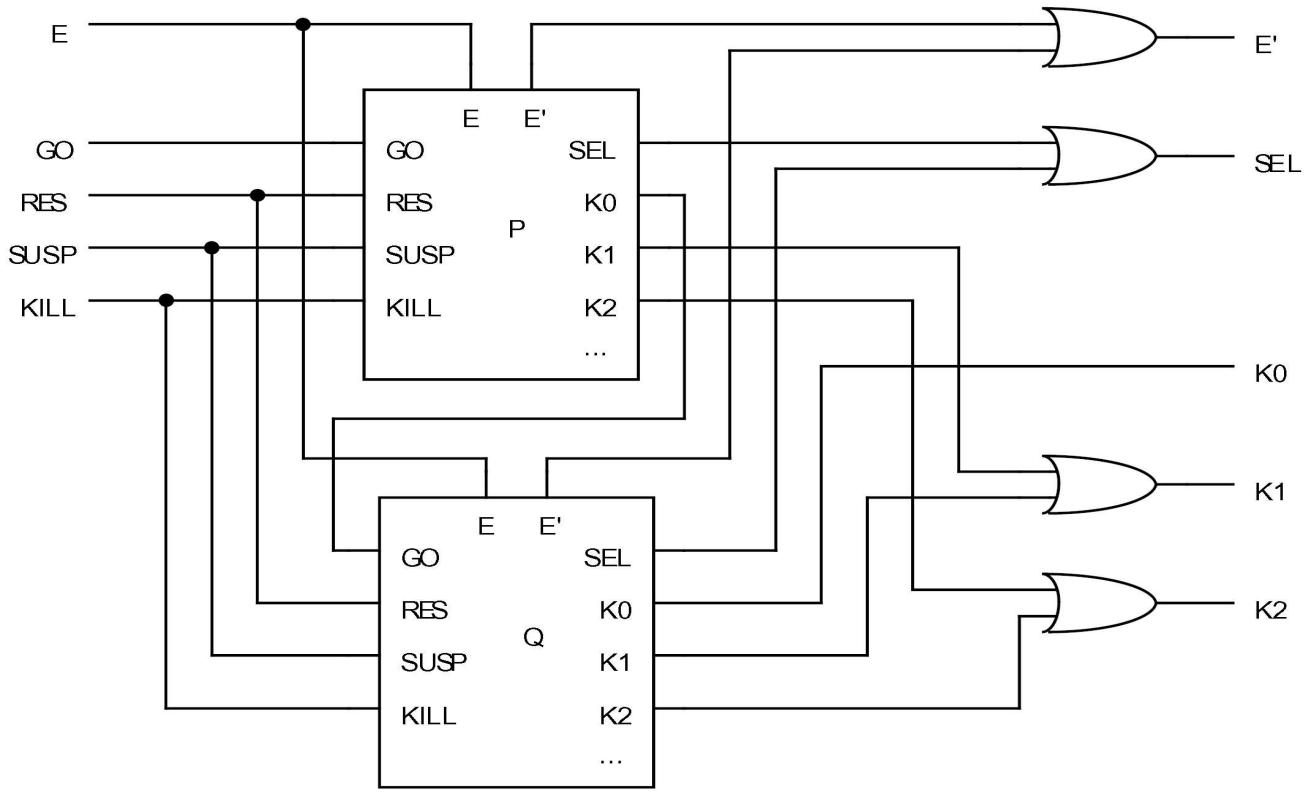
Translating the Esterel Kernel

- $!s$:



Translating the Esterel Kernel

- $p; q$:



Translating the Esterel Kernel

- $s?p, q$:

Translating the Esterel Kernel

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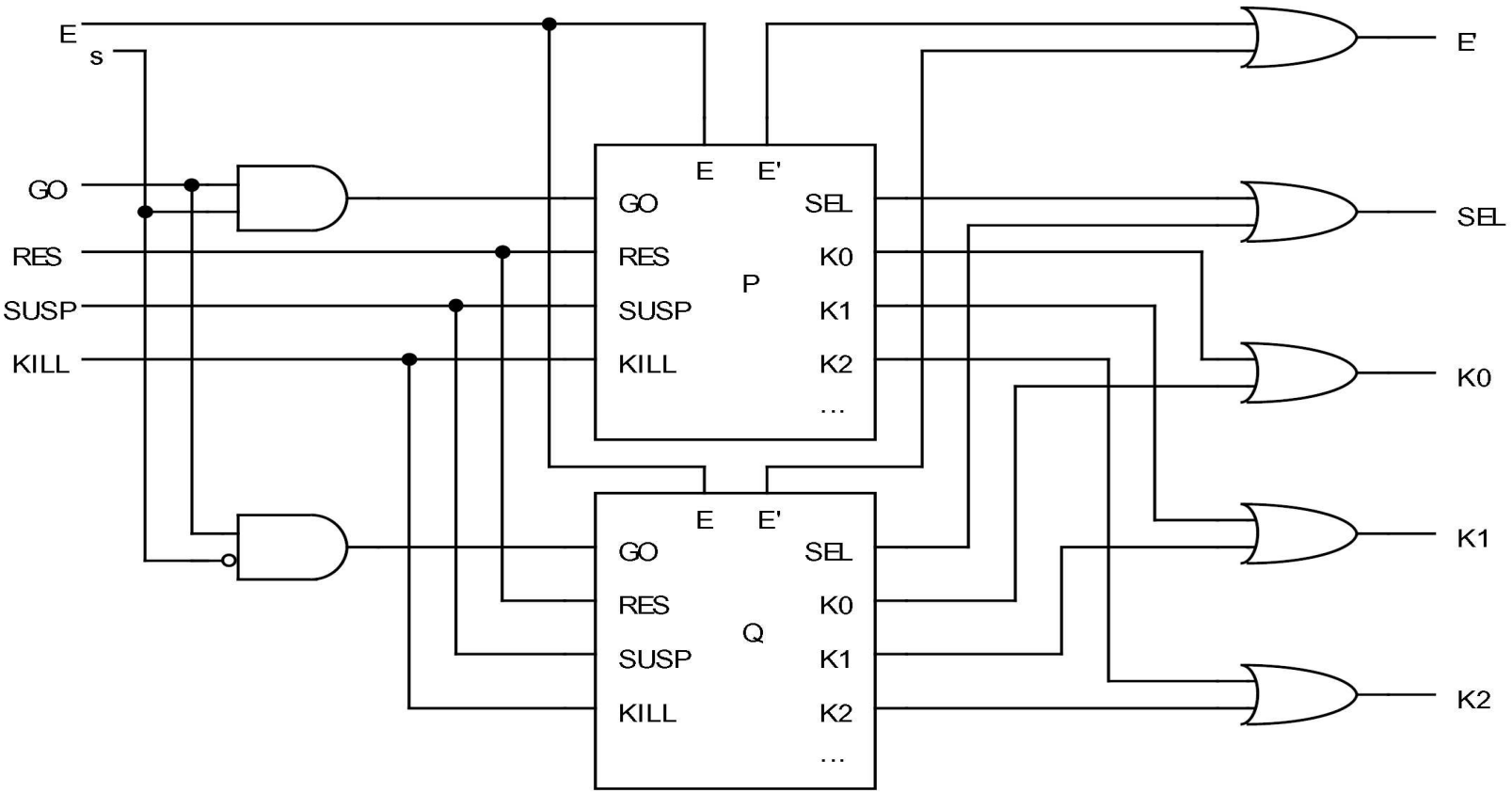
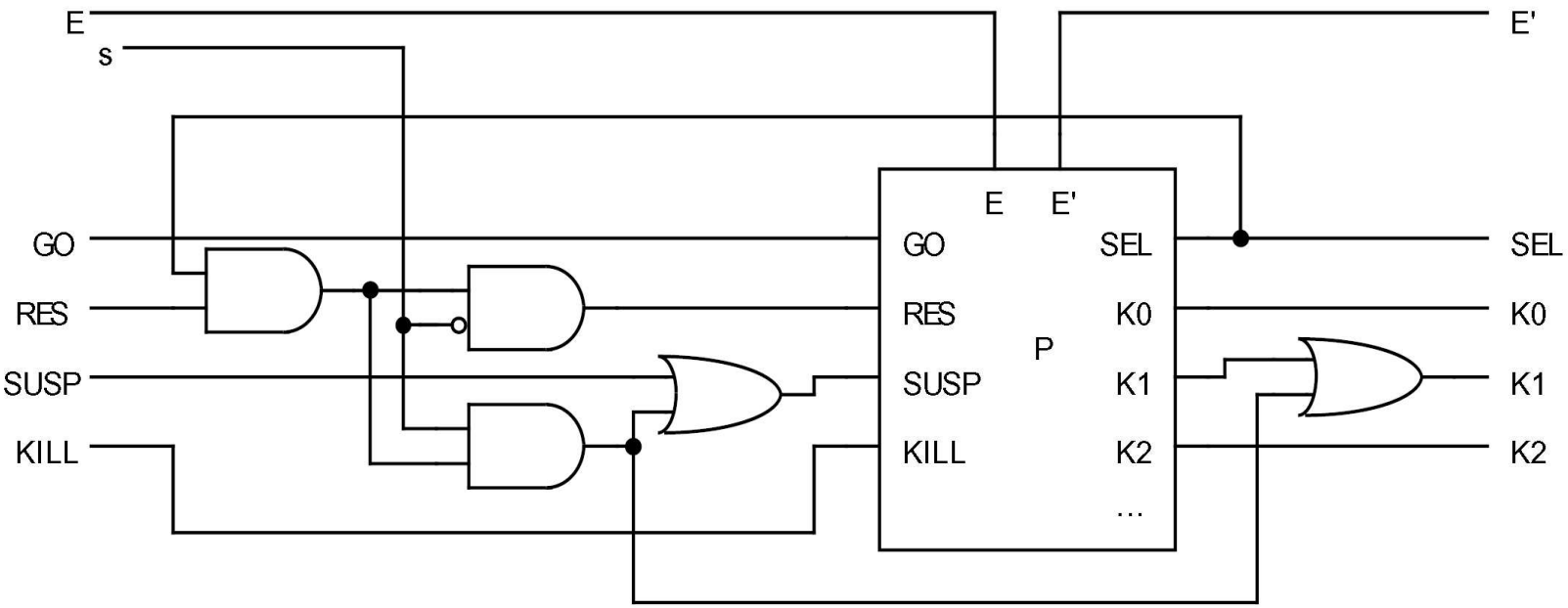


Translating the Esterel Kernel

- $s \supset p$:

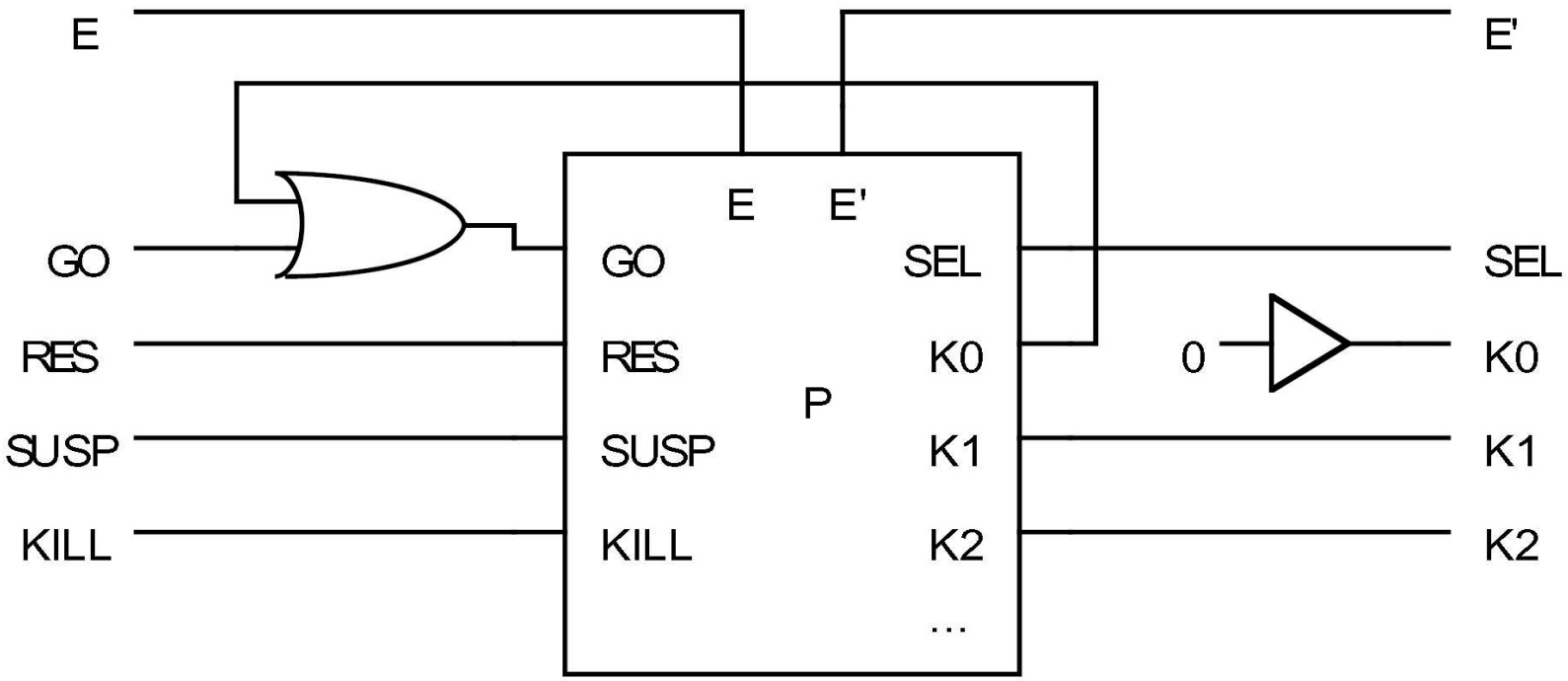


Translating the Esterel Kernel

- $p*$:

Translating the Esterel Kernel

- $p*$:

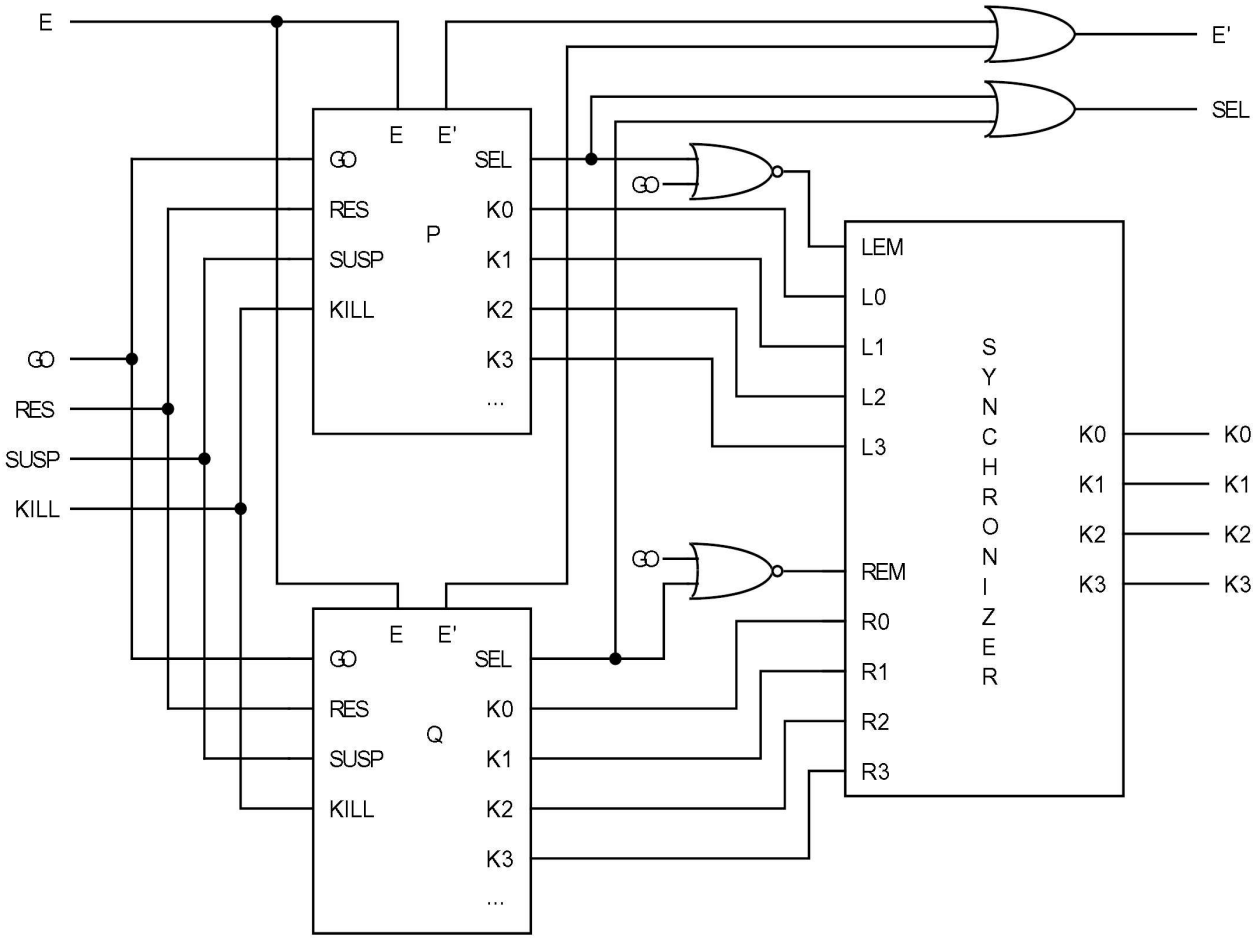


Translating the Esterel Kernel

- $p \parallel q$:

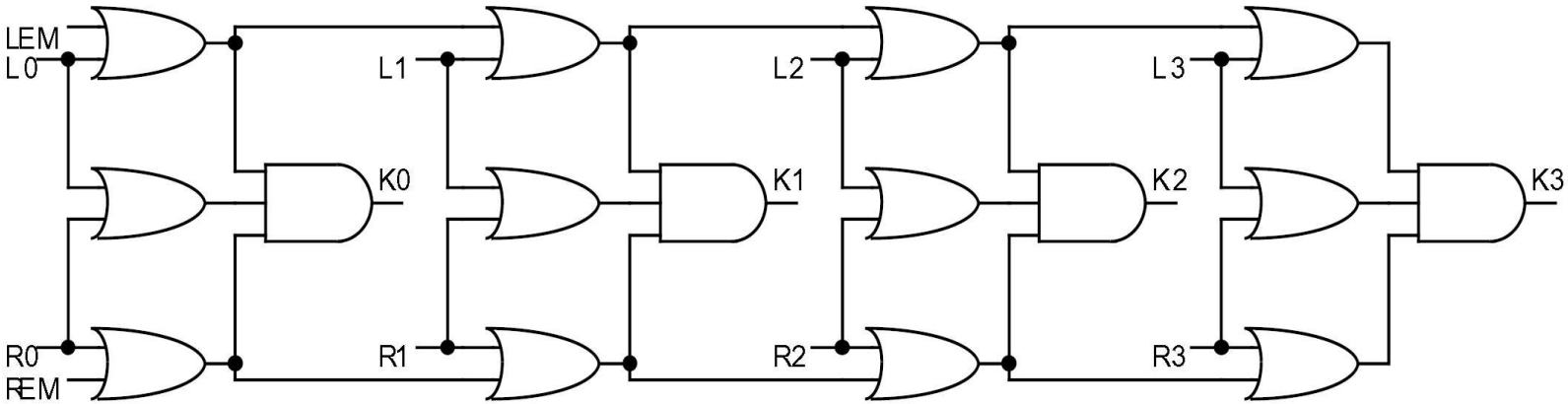
Translating the Esterel Kernel

- $p \parallel q$:



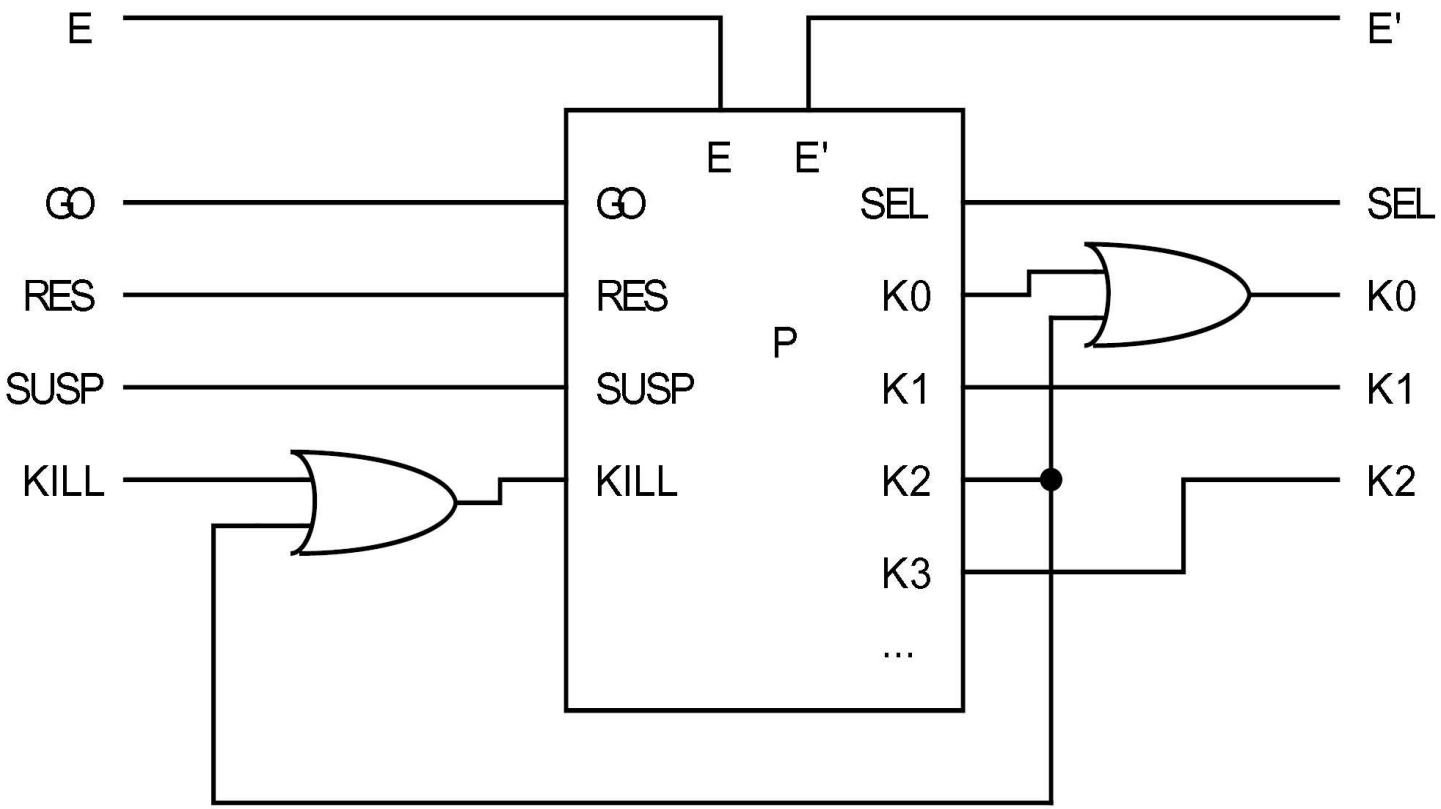
Translating the Esterel Kernel

- $p \parallel q$ (contd):
  - The synchronizer computes the maximum of the completion codes
  - Implemented with this (constructive) circuit:



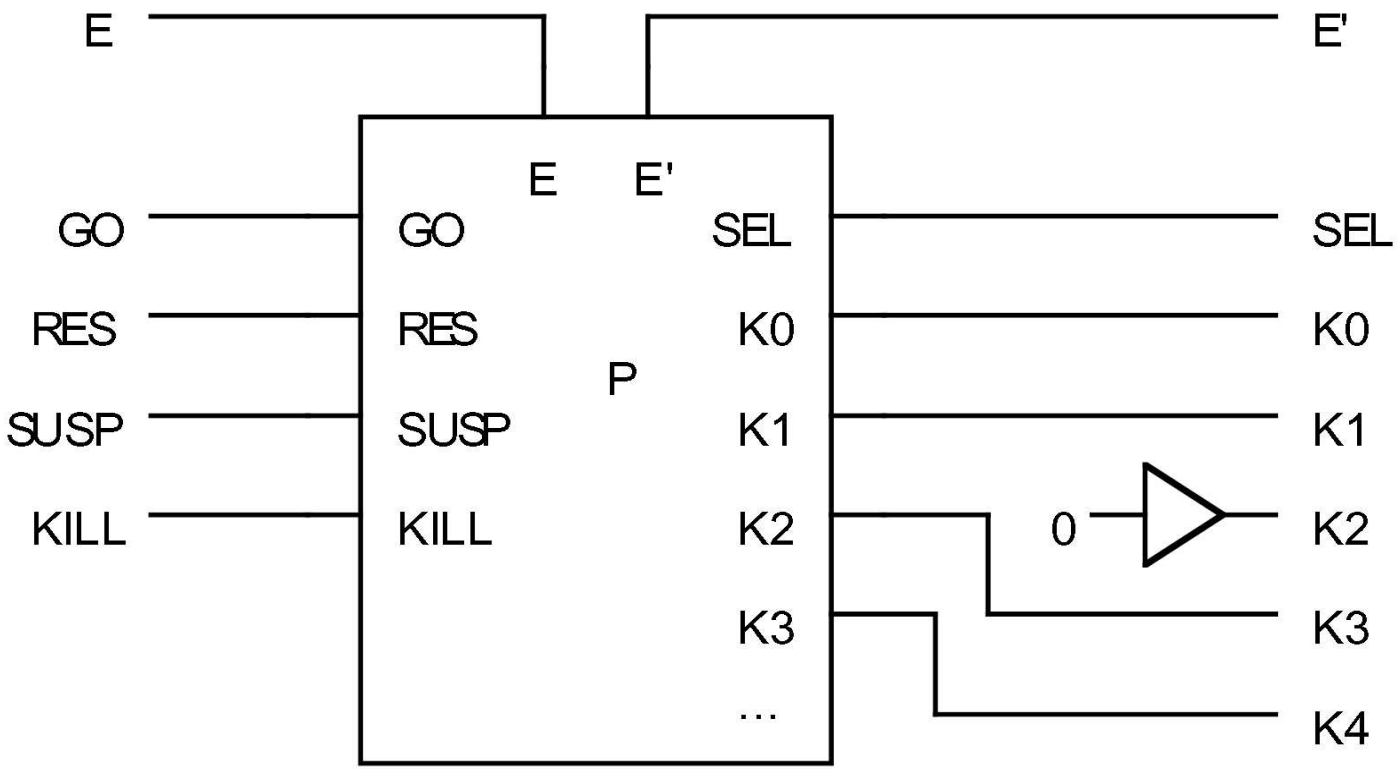
Translating the Esterel Kernel

- $\{p\}$:



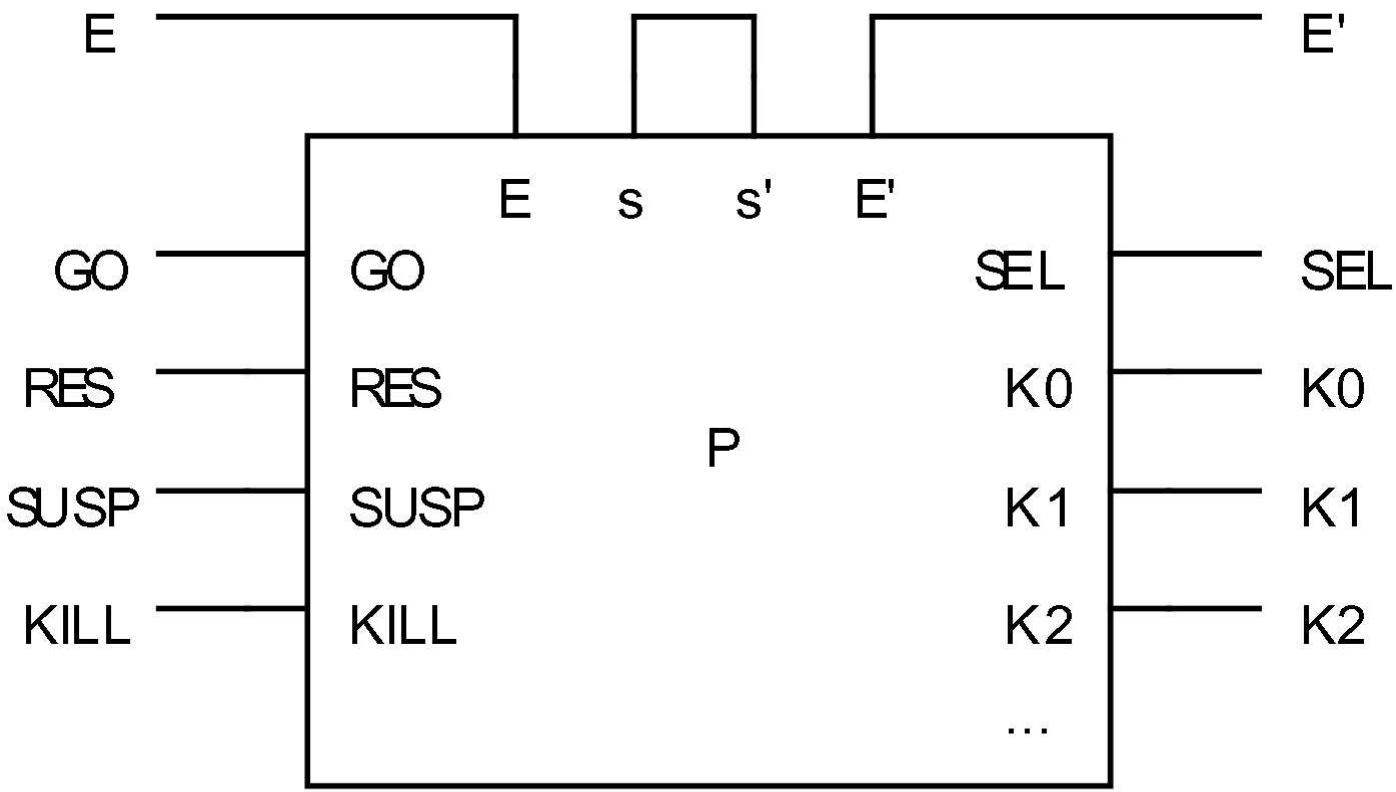
Translating the Esterel Kernel

- $\uparrow p$:



Translating the Esterel Kernel

- $p \backslash s$:



Example

```
module P2:
signal S in
  emit S;
  present O then
    present S then
      pause
    end present;
    emit O
  end present
end signal
```

Example

```
module P2:
signal S in
  emit S;
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    present S then
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    emit O
  end present
end signal
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≡

circuit C2:

$B = \neg\, \mathrm{REG}(1)$ // *Boot*

$S = B$

$R = \mathrm{REG}(B \wedge O \wedge S)$ // *pause*

$O = (B \wedge O \wedge \neg S) \vee R$

$K0 = (B \wedge \neg O) \vee (B \wedge O \wedge \neg S) \vee R$

$K1 = B \wedge O \wedge S$

Example

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module P2:
signal S in
  emit S;
  present O then
    present S then
      pause
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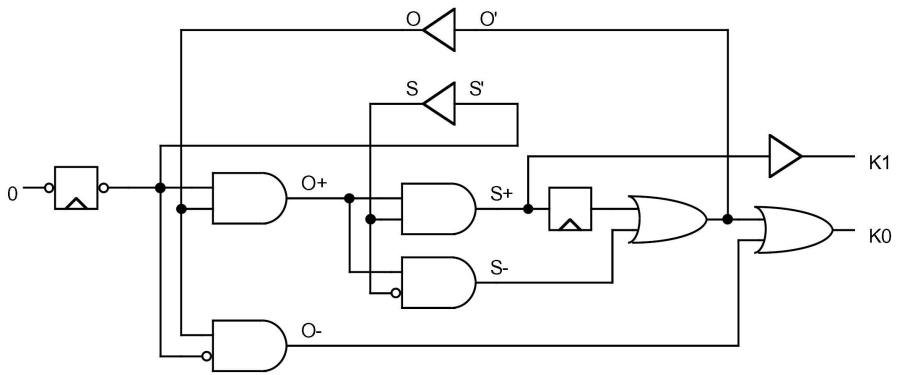

To Go Further

- Gérard Berry, The Constructive Semantics of Pure Esterel, Draft book, current version 3.0, Dec. 2002, Chapters 10 and 11,
  `http://www-sop.inria.fr/members/Gerard.Berry/Papers/EsterelConstructiveBook.zip`