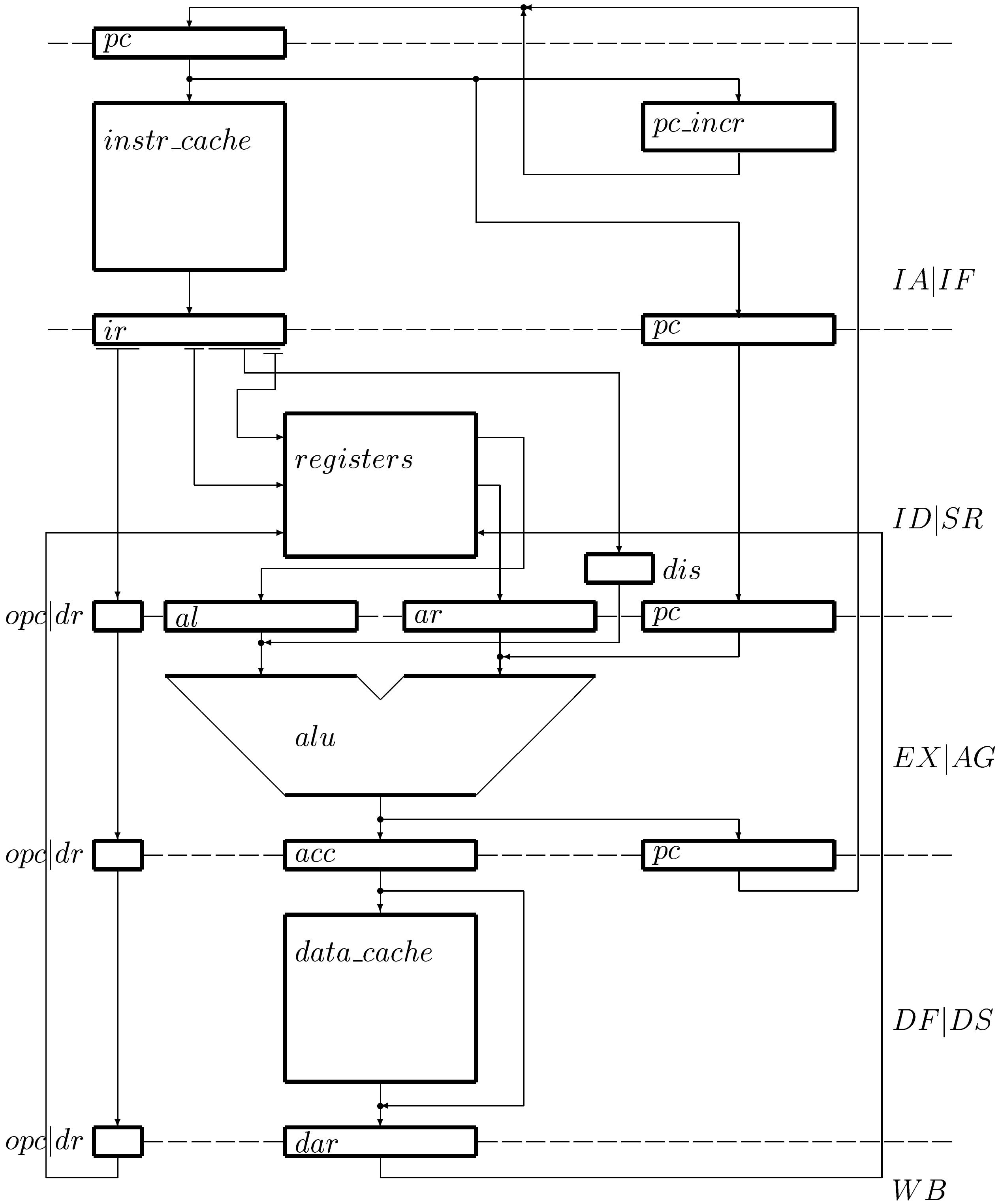
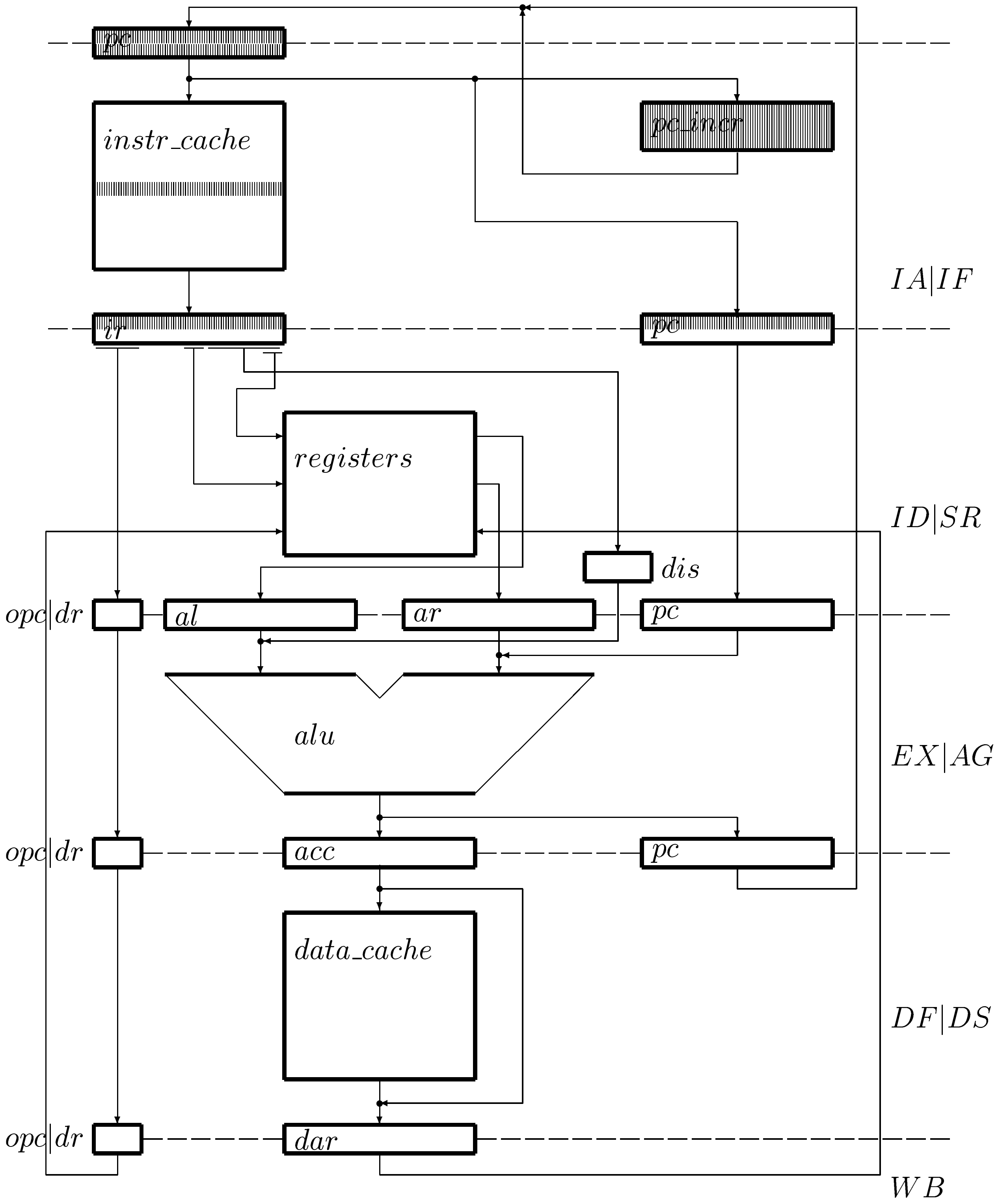
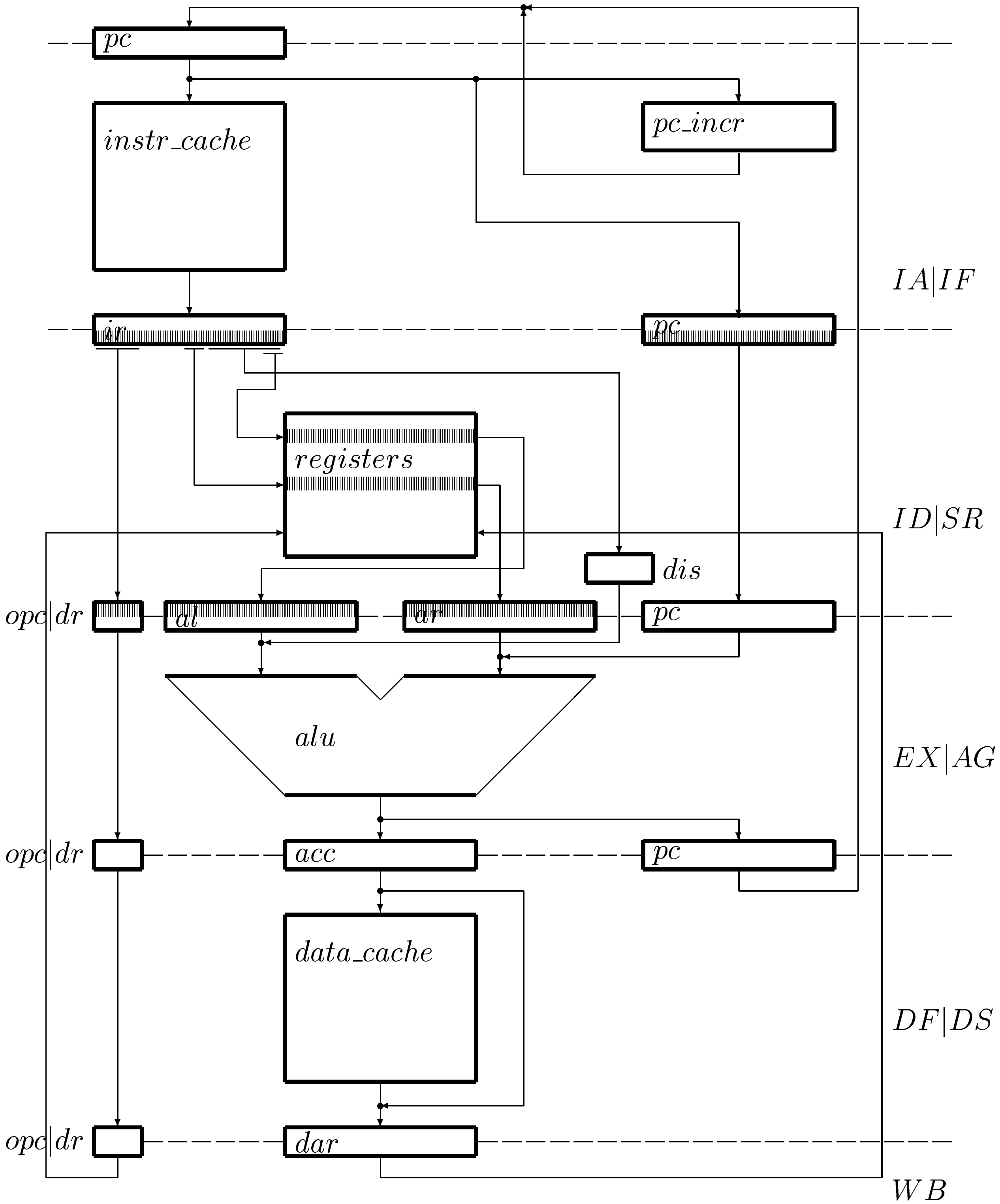


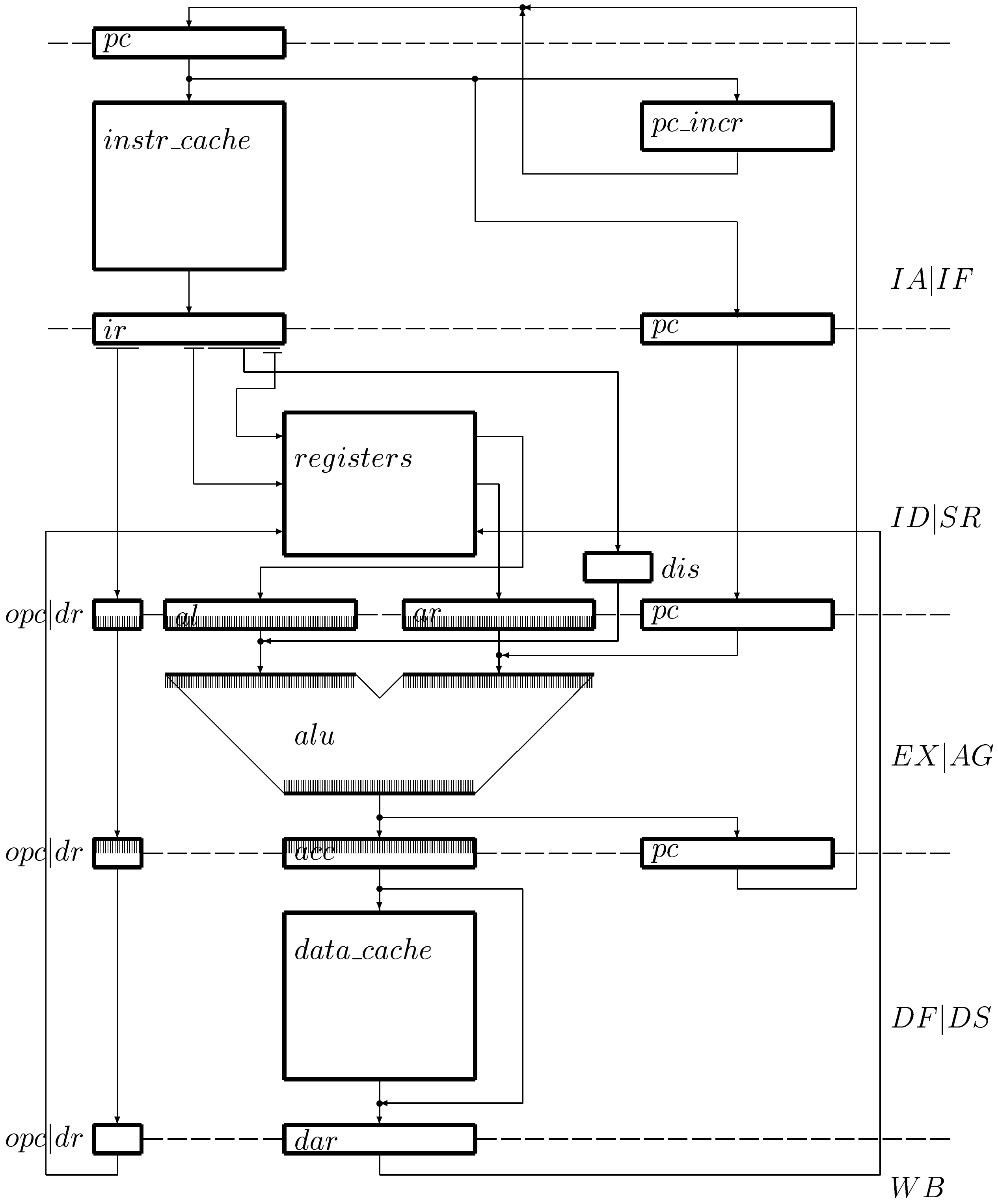
A five stages pipeline [1]



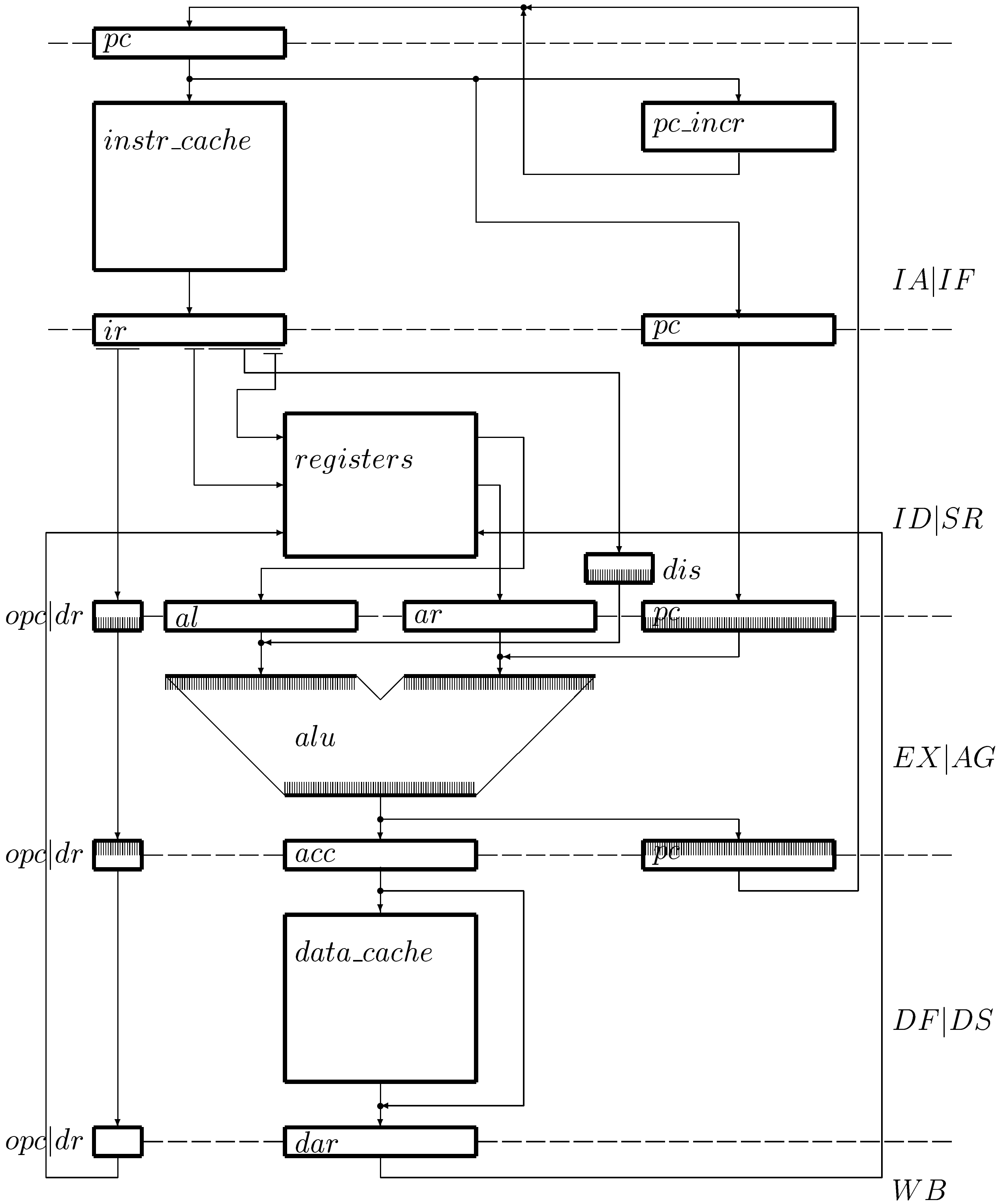
Instruction address / fetch phase active



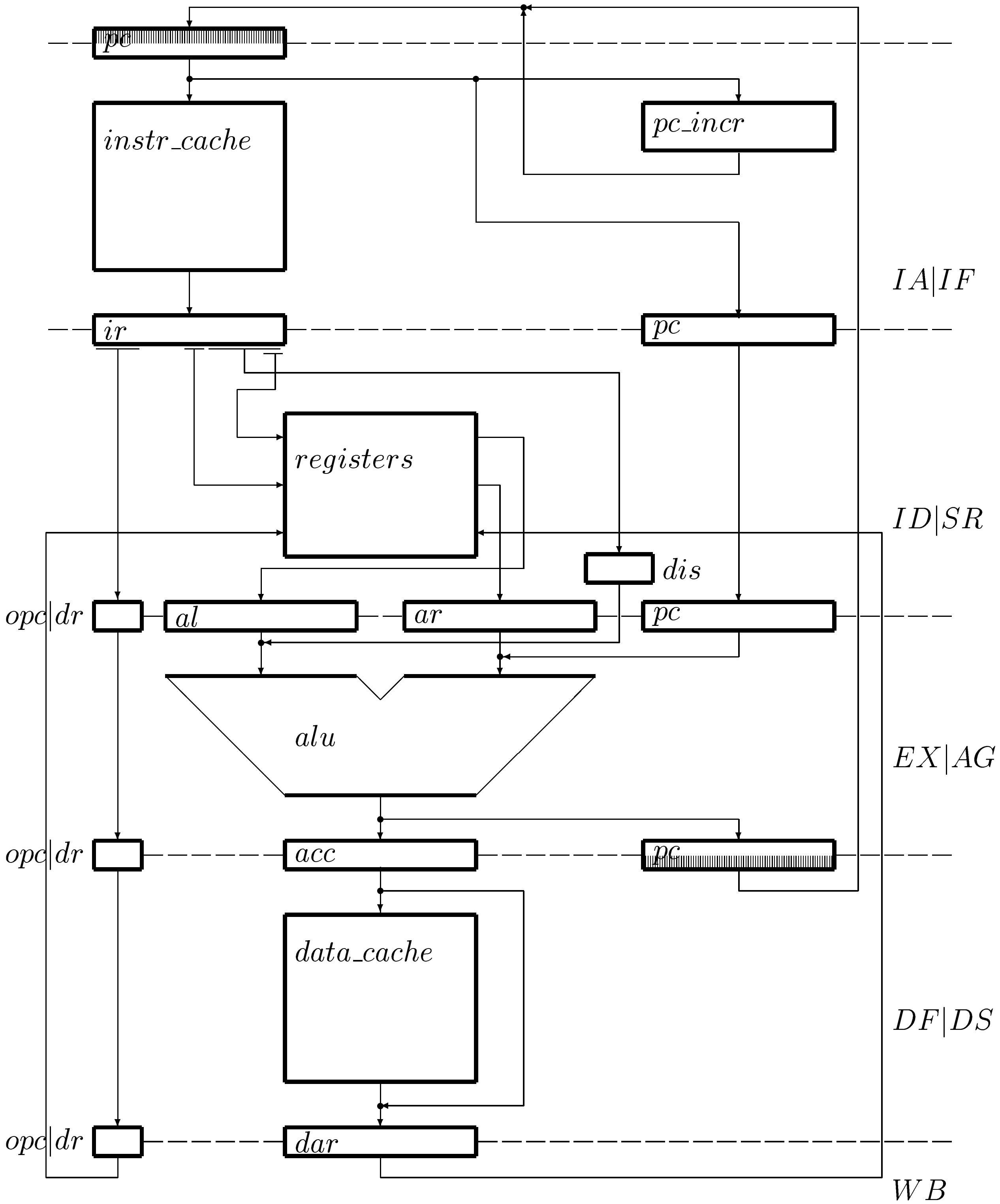
Instruction decode / source reg access phase active



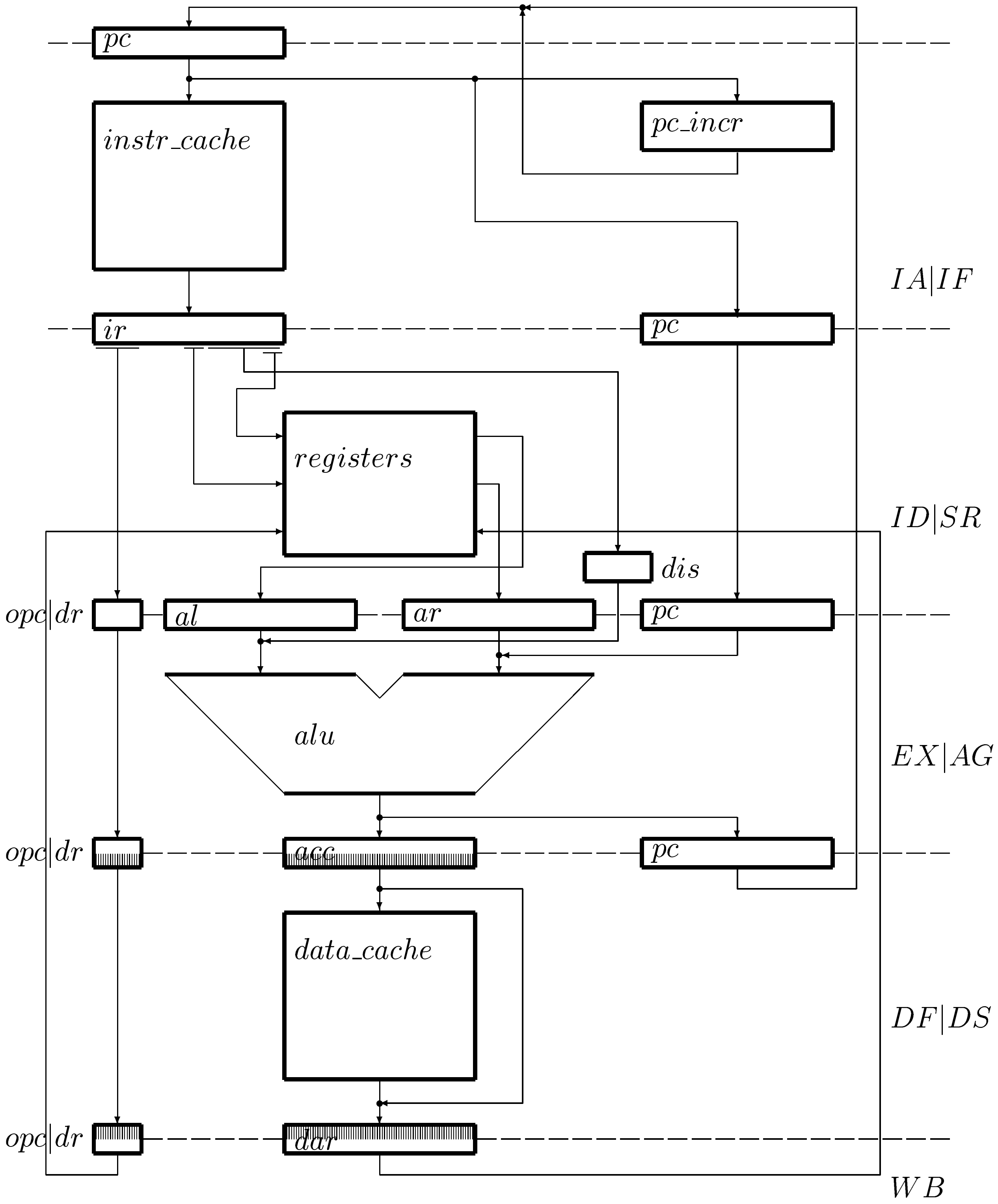
Instruction execution / address generation phase active



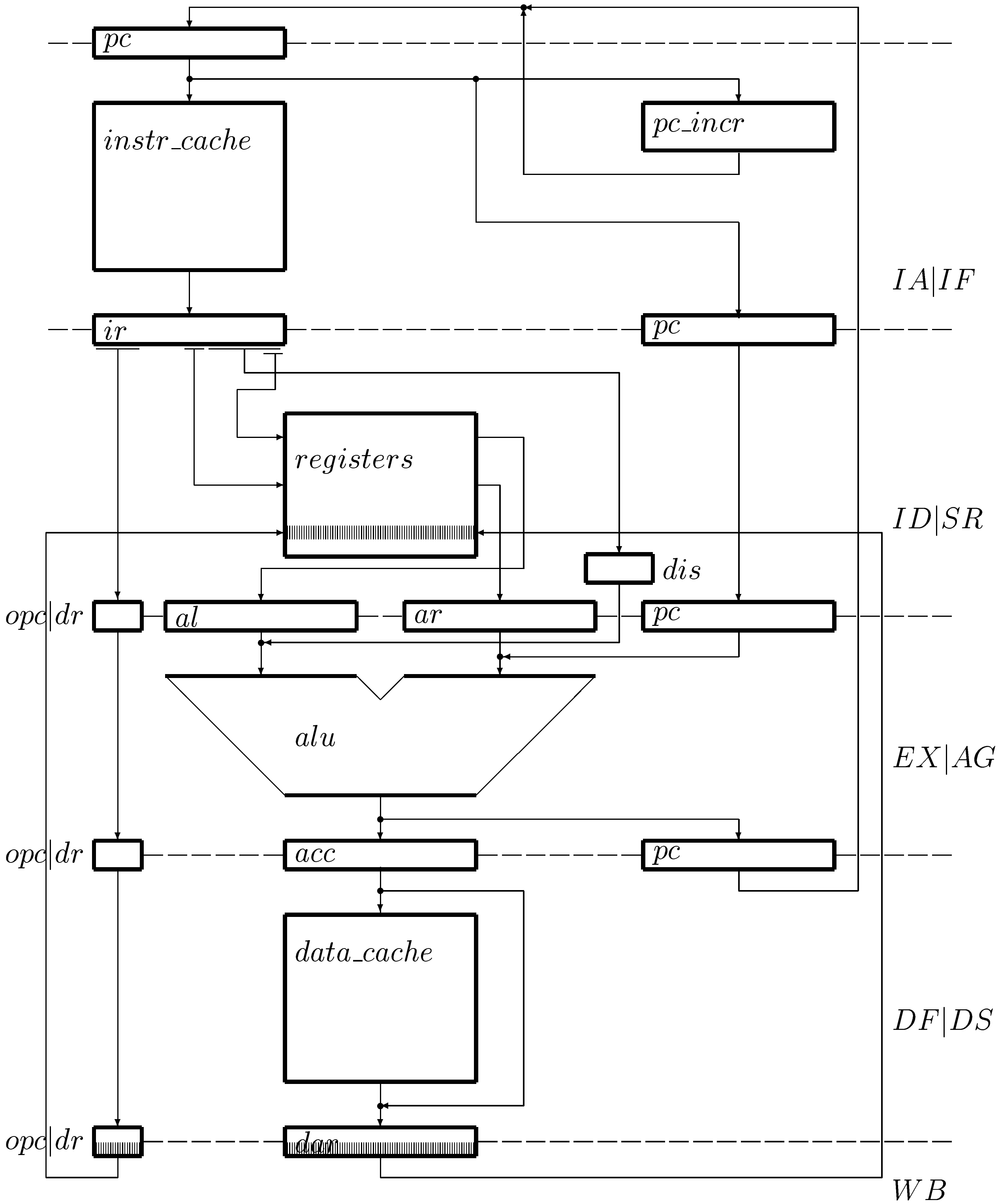
Branch target computation phase active



Branch target write back phase active



DATA FETCH / DATA STORE PHASE ACTIVE



Data write back phase active